

INF3410/4411, Fall 2018

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Excerpt of Sedra/Smith Chapter 8: Differential and Multistage
CMOS Amplifier Basics

Content

The MOS Differential Pair (book 8.1)

Common Mode Rejection and Random DC offset (book 8.3-8.4)

Current Mirror Load (book 8.5)

Multi Stage Amplifiers (book 8.6)

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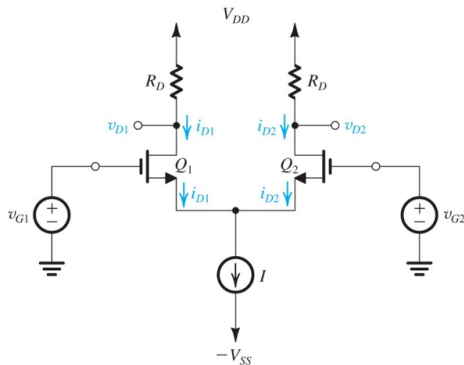
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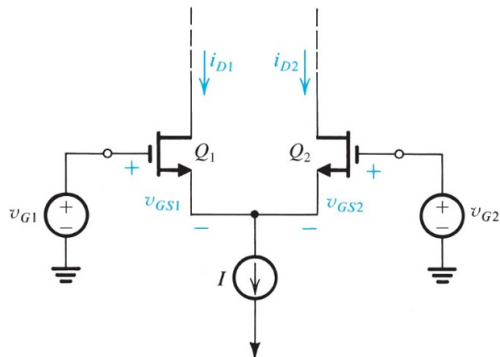
Multi Stage Amplifiers (book 8.6)

The differential pair with resistive loads

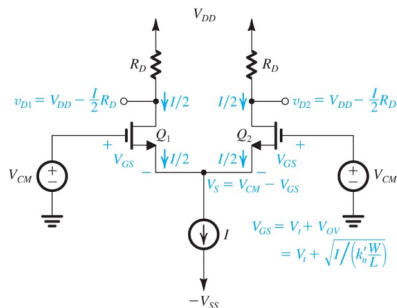


The resistors turn i_d linearly into voltage

Easier (in my opinion): look simply at i_d



Analysis for Common Mode Input



With ideal current source:
 common mode voltage V_{CM} has
 no effect, but beware the range of
 operation!!!

$$V_{CMmax} = V_t + V_{DD} - \frac{I}{2} R_D \quad (8.7)$$

$$V_{CMmin} = -V_{SS} + V_{CS} + V_t + V_{OV} \quad (8.8)$$

(Note that the book always
 writes $-V_{SS}$ at the actual
 terminal, i.e. always expresses
 V_{SS} as a positive number...)

Large Signal, Weak Inversion

Simpler analysis in weak inversion:

$$I_b = I_1 + I_2 = I_S e^{\frac{-V_t - nV_S}{nV_T}} \left(e^{\frac{V_1}{nV_T}} + e^{\frac{V_2}{nV_T}} \right)$$

$$I_{out} = I_1 - I_2 = I_S e^{\frac{-V_t - nV_S}{nV_T}} \left(e^{\frac{V_1}{nV_T}} - e^{\frac{V_2}{nV_T}} \right)$$

$$\frac{I_{out}}{I_b} = \frac{e^{\frac{V_1}{nV_T}} - e^{\frac{V_2}{nV_T}}}{e^{\frac{V_1}{nV_T}} + e^{\frac{V_2}{nV_T}}}$$

$$I_{out} = I_b \frac{e^{\frac{V_1}{nV_T}} - e^{\frac{V_2}{nV_T}}}{e^{\frac{V_1}{nV_T}} + e^{\frac{V_2}{nV_T}}} = I_b \tanh \frac{V_1 - V_2}{2nV_T}$$

Small Signal, Weak Inversion

Since the slope of $\tanh x$ for $x = 0$ is 1, the slope of $I_b \tanh \frac{\Delta V}{2nV_T}$ with respect to ΔV (the transconductance g of this transamp) is:

$$g = \frac{I_b}{2nV_T}$$

Large Signal, Strong Inversion (1/2)

$$I_b = I_1 + I_2 = k_n(V_{OV1}^2 + V_{OV2}^2)$$

$$I_{out} = I_1 - I_2 = k_n(V_{OV1}^2 - V_{OV2}^2)$$

$$\frac{I_{out}}{I_b} = \frac{V_{OV1}^2 - V_{OV2}^2}{V_{OV1}^2 + V_{OV2}^2}$$

$$I_{out} = I_b \frac{V_{OV1}^2 - V_{OV2}^2}{V_{OV1}^2 + V_{OV2}^2}$$

Large Signal, Strong Inversion (2/2)

Rewrite with $\hat{V}_{OV} = \frac{V_{OV1} + V_{OV2}}{2}$ and $\Delta V_{OV} = V_{OV1} - V_{OV2}$

$$I_{out} = I_b \frac{2\Delta V_{OV} \hat{V}_{OV}}{\frac{1}{2} (\Delta V_{OV}^2 + (2\hat{V}_{OV})^2)}$$

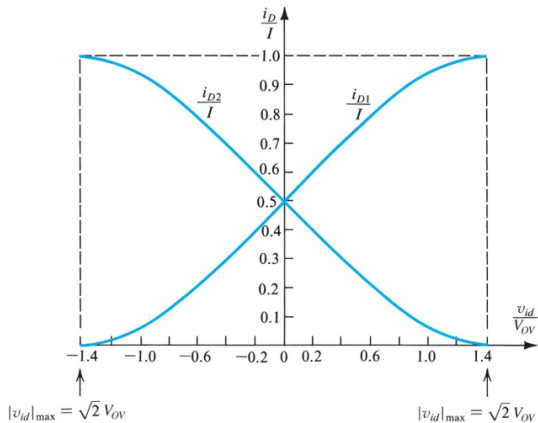
Note that this is not yet a closed solution as in the large signal world V_S , and thus \hat{V}_{OV} depends on ΔV_{OV} .

Extrema where one transistor conducts the entire I_B is where $\Delta V_{OV} = 2\hat{V}_{OV}$ (since then one branch has $V_{OV2} = 0$) and $I_B = k_n \Delta V_{OV}^2$. It follows that:

$$\Delta V_{OV} = \sqrt{\frac{I_B}{k_n}} = \sqrt{2} V_{OV}$$

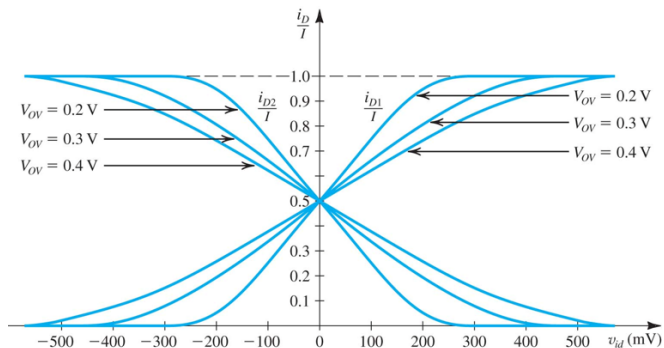
Where like in the book V_{OV} is the overdrive voltage for $\Delta V_{OV} = 0$

Normalized I/V Curves and Ranges

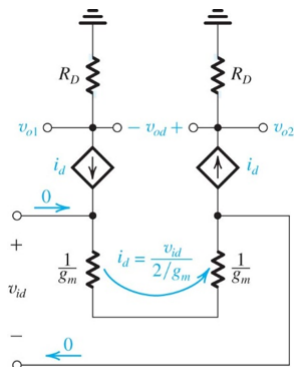


I/V Curves for different V_{OV} respectively $\frac{W}{L}$

(This is only valid for strong inversion)



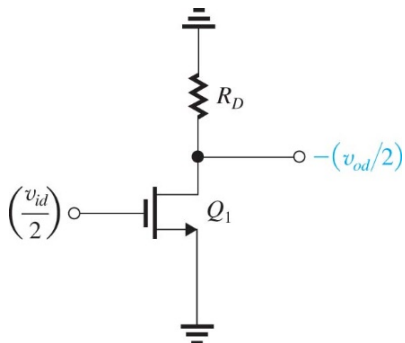
Small Signal Analysis on the Half Circuit (1/2)



(b)

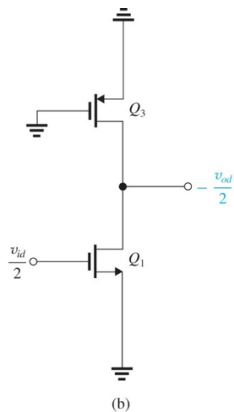
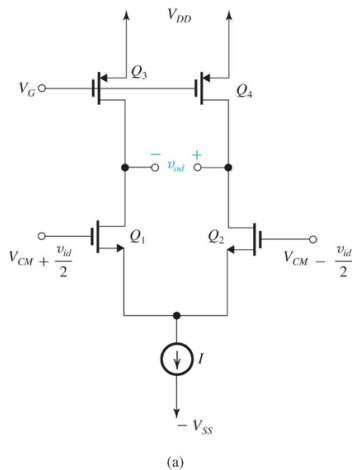
Assuming a 'balanced' input, i.e. $v_{g1} = -v_{g2} = \frac{v_{id}}{2}$. This results in a virtual small signal Gnd at the source of the transistors.

Small Signal Analysis on the Half Circuit (2/2)

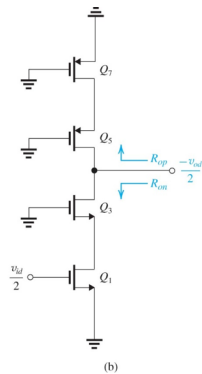
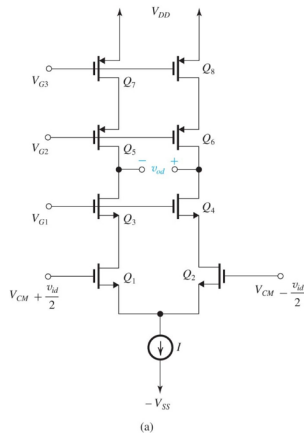


Thus one can look at the branches individually: It's the good old common source amp.

Current Source Load Differential Amplifier



Cascode Differential Amplifier



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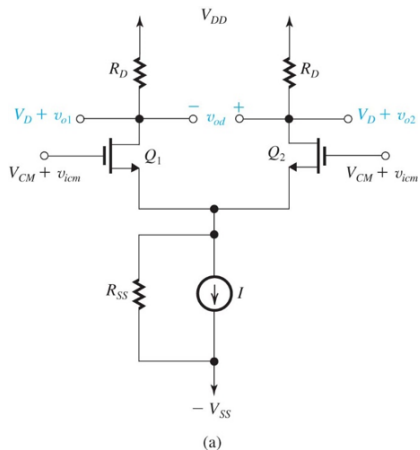
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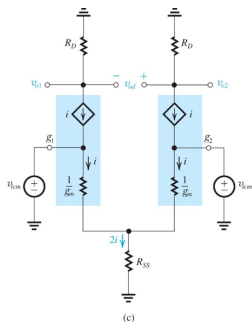
Current Mirror Load (book 8.5)

Multi Stage Amplifiers (book 8.6)

Common Mode Rejection



Common Mode Rejection



$$v_{icm} = \frac{i}{g_m} + 2iR_{SS}$$

$$i = \frac{v_{icm}}{\frac{1}{g_m} + 2R_{SS}} \approx \frac{v_{icm}}{2R_{SS}}$$

And R_D converts i into the two output voltages v_{o1} and v_{o2} . Note that the *difference* of currents is still 0, i.e. not affected by the common mode input. However, since a change in i , respectively a change in I_b , affects the transconductance, v_{icm} will influence the output difference if the differential input is not zero, and mismatch will lead to common mode gain, i.e. a DC offset with zero input difference that varies with v_{icm} .

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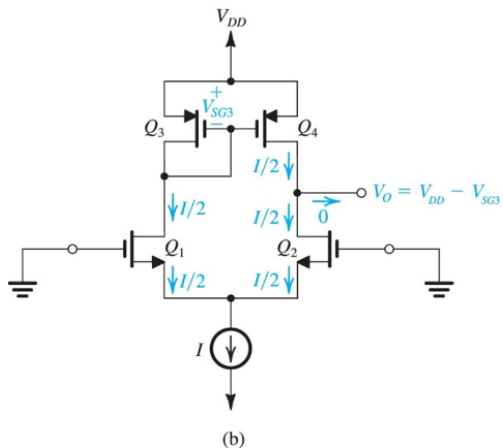
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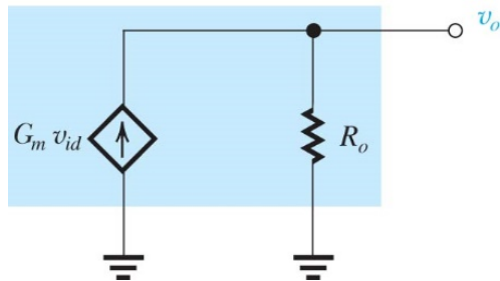
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Systematic DC offset with current mirror load

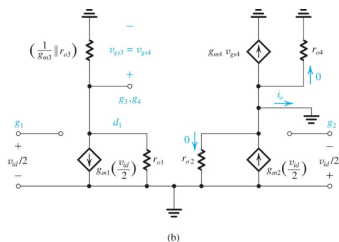


Output equivalent circuit



$$A_d = \frac{v_o}{v_{id}} = G_m R_o = g_{m1,2}(r_{o2} || r_{o4})$$

A more careful deduction of G_m

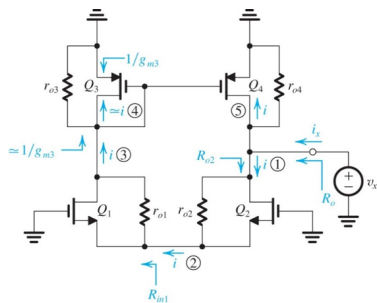


$$i_o = g_{m2} \frac{v_{id}}{2} - g_{m4} v_{gs4} \quad (8.132)$$

$$\begin{aligned} v_{gs3} &= -g_{m1} \frac{v_{id}}{2} \left(\frac{1}{g_{m3}} \parallel r_{o3} \parallel r_{o1} \right) \\ &\approx -\frac{g_{m1}}{g_{m3}} \frac{v_{id}}{2} \quad (8.134) \end{aligned}$$

$$i_o \approx g_m v_{id} \Rightarrow G_m = g_m$$

A more careful deduction of R_o



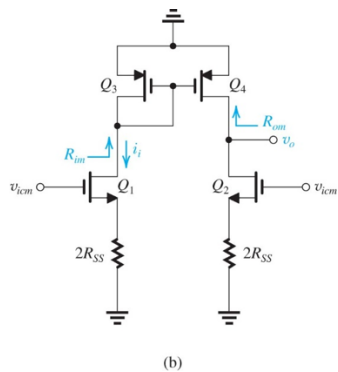
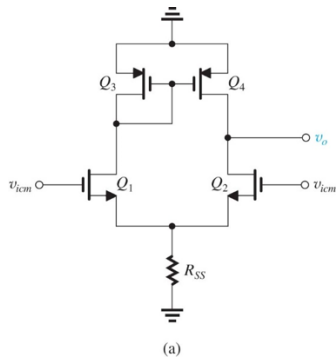
$$i = \frac{v_x}{R_{o2}}$$

$$R_{in1} = \frac{r_{o1} + R_L}{g_{m1} r_{o1}} \approx \frac{1}{g_{m1}}$$

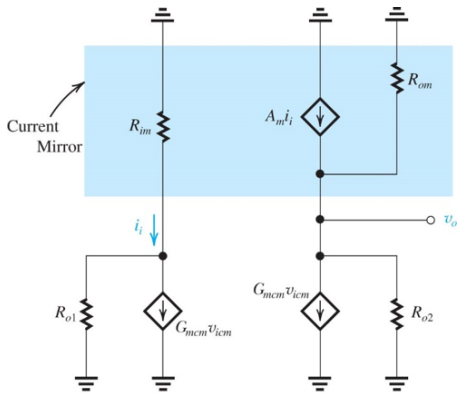
$$R_{o2} = R_{in1} + r_{o2} + g_{m2} r_{o2} R_{in1}$$

$$\approx 2r_{o2} \quad (8.135)$$

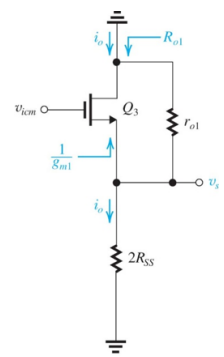
Common Mode Gain (1/2)



Common Mode Gain (2/2)

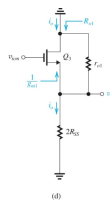
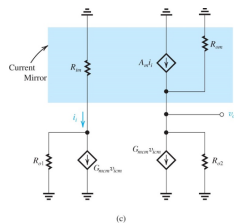


(c)



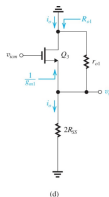
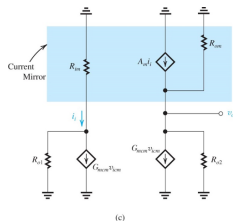
(d)

For General Current Gain



$$A_{cm} = \frac{v_o}{v_{icm}} = -(1 - A_m)G_{mcm}(R_{om} || R_{o2})$$

For Simple Current Mirror



$$A_m i_i = v_{gs3} g_{m3} \quad v_{gs3} = i_i R_{im} \quad R_{im} = \frac{1}{g_{m3}} \parallel r_{o3}$$

$$A_m = \frac{1}{1 + \frac{1}{g_{m3} r_{o3}}}$$

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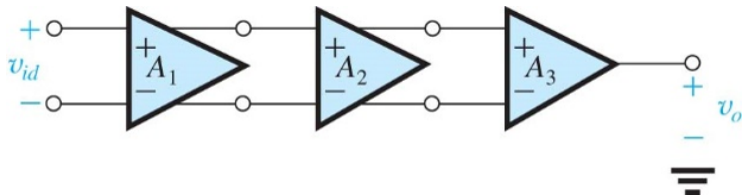
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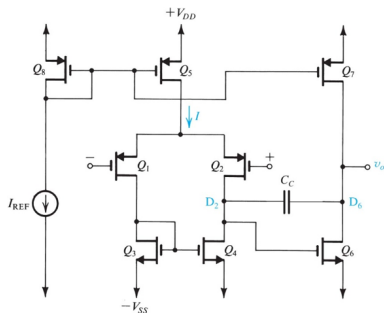
Multi Stage Amplifiers (book 8.6)

Internally All Differential Example



Has some advantages, foremost a better CMRR. And with single ended stages you have to care about 'hitting' the right input DC level of the next stage.

Two Stage CMOS op-amp Example



$$A = A_1 A_2 = g_{m1}(r_{o2} || r_{o4}) g_{m6}(r_{o6} || r_{o7})$$

$$\frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$$