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Introduction to the Zynq SOC

INF3430/INF4431

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First hour – Zynq architecture

- Computational platforms
- Design flow
- System overview
- PS
  - APU
  - IOP
    - MIO
    - EMIO
- Datapath
- PS/PL interconnect
- PL
  - Zynq family
- Zynq boards

Second hour – AXI interface

- Overview
- Axi4-stream
- Axi4-lite
- Axi4

Computational platforms

Sequential:

CPU:

- General purpose
- Easy to implement
- High flexibility and compatibility
- Many accelerated functions

DSP:

- Specific purpose
- Few but powerful accelerated functions

Parallel:

GPU:

- Parallel floating point
- Easy/cheap development
- Higher compatibility
- High flexibility
- Low cost

FPGA:

- Parallel integer
- Custom hardware
- Low power
- Low latency (RT)
- High security

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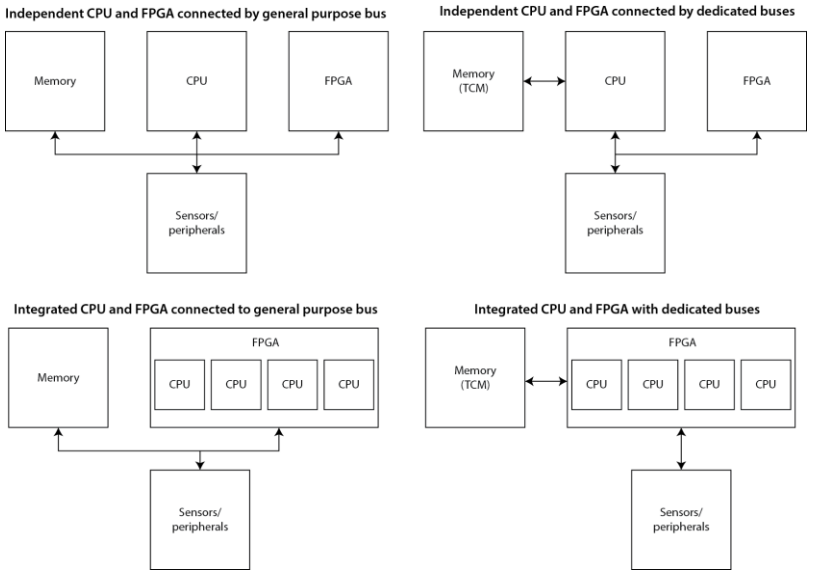
CPU and FPGA



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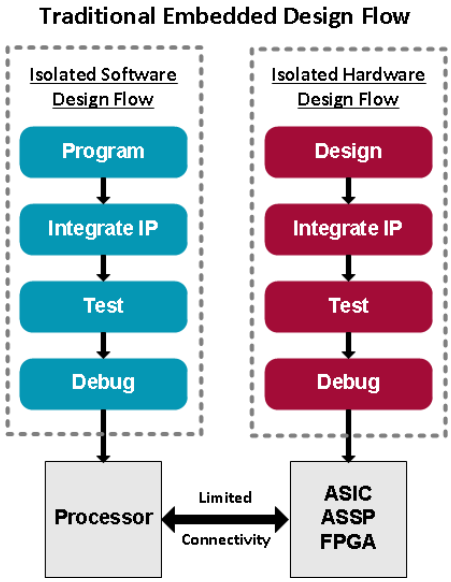
Design flow

Traditional design flow:

- Different teams
- Isolated design flows
- Separate testing
- Limited interconnect



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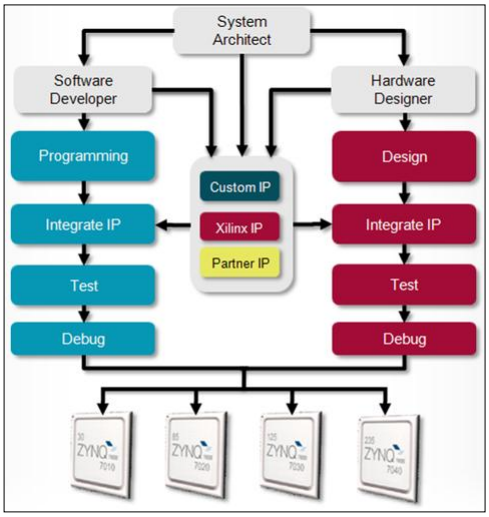
Design flow

Improved design flow:

- Cooperation throughout the process
- Extensive use of IPs



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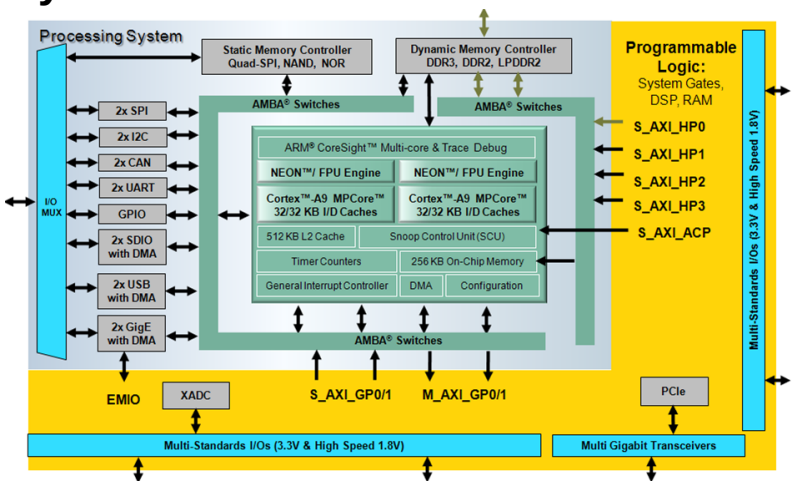
System overview



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PS

- Consists of the following 4 units:
  - Application Processor Unit (APU)
  - I/O Peripherals (IOP)
  - Datapath (Interconnects and interfaces)
  - Memory resources and caches
- Includes a Dual Arm Cortex A9 Processor
  - Up to 1GHz
  - Up to 1333Mb/s DDR3 interface

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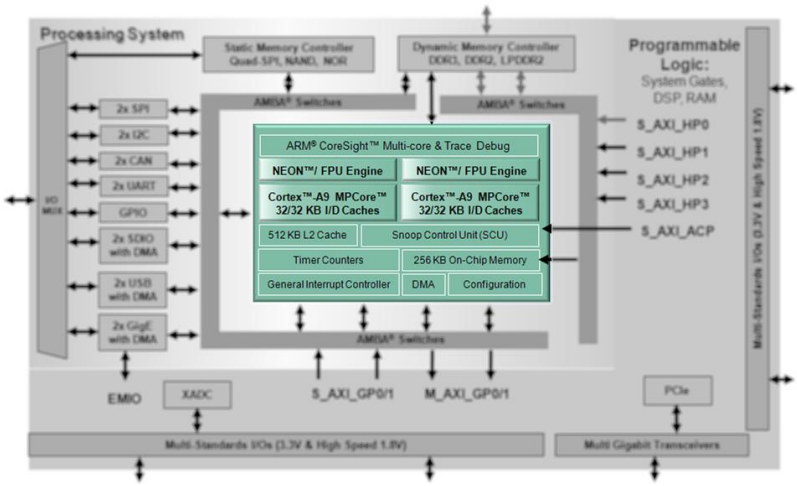
APU



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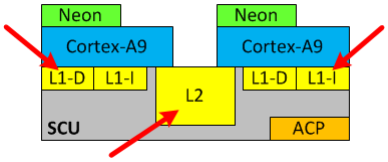
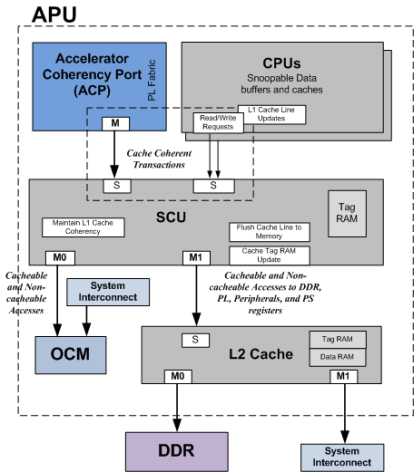
APU

- Range of connections to memory and the rest of the system
- Different levels of caches and memory





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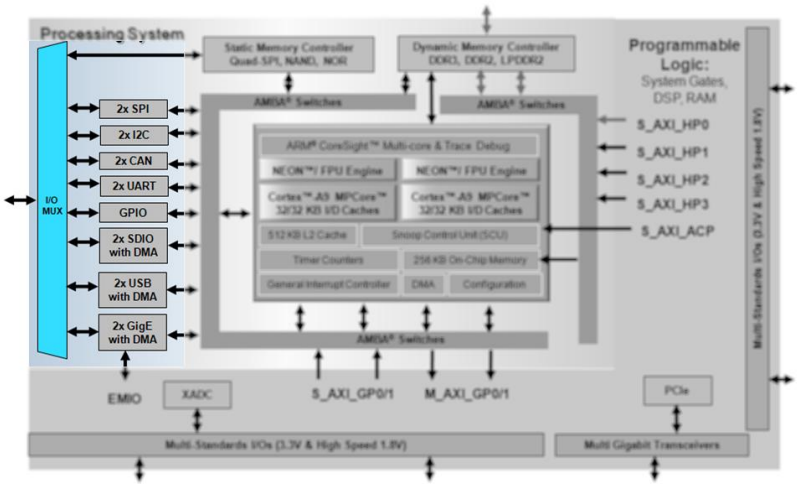
IOP



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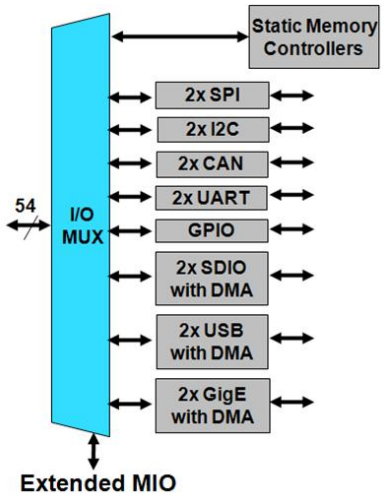
IOP – MIO

- Two blocks each except GPIO
- Four 32-bit GPIO blocks
  - 54 through MIO
  - 64 though EMIO
- Separate DMAs for:
  - USB
  - SD/SDIO
  - Ethernet



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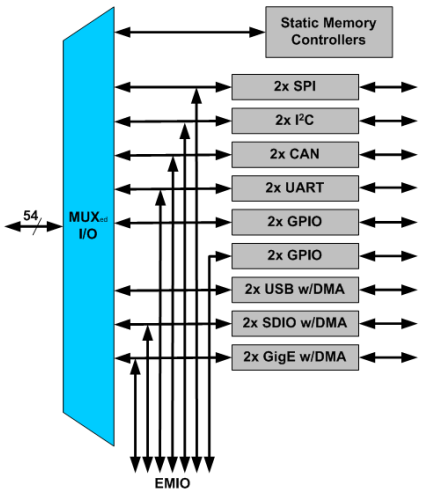
IOP – EMIO

- Connects to PL
- Configured with Vivado IP Integrator
- Two IO banks with 1.8V, 2.5V or 3.3V



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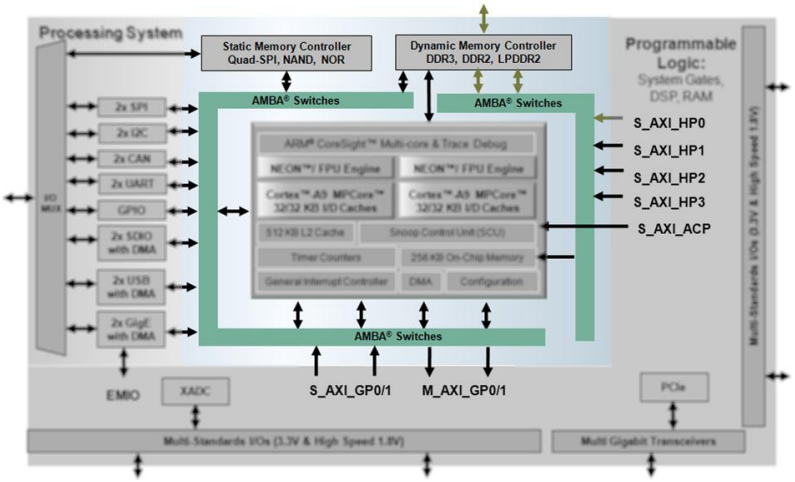
Datapath and memory



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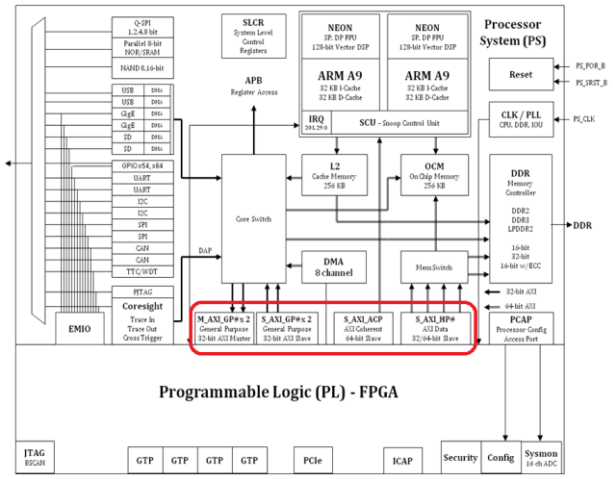
PS/PL Interfaces – AXI3



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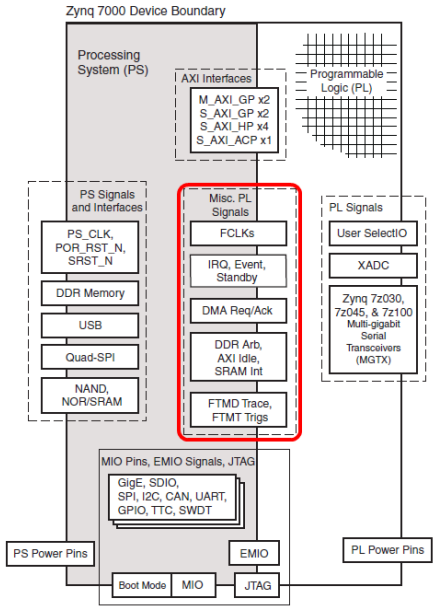
PS/PL Interfaces

- Also misc signals
  - Clock/reset
  - Interrupts
  - DMA
  - Debug/trace
  - EMIO



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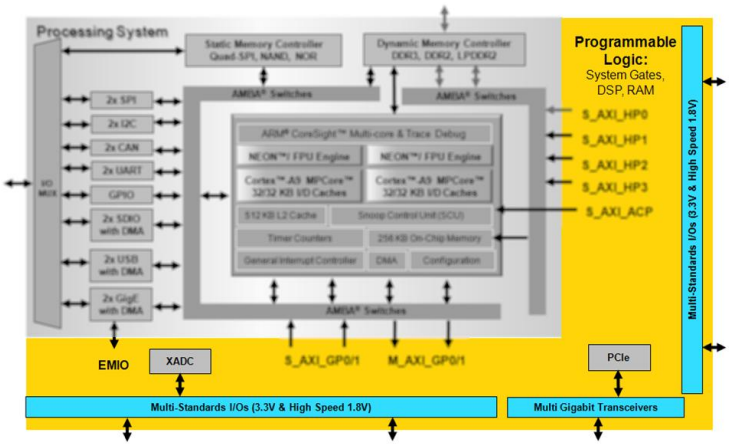
PL



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The Zynq Family

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The Zynq Family

Zynq-7000 All Programmable SoC

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	866 MHz			Up to 1 GHz [1]			
	L1 Cache	32 KB Instruction, 32 KB Data per processor						
	L2 Cache	512 KB						
	On-Chip Memory	256 KB						
	External Memory Support [2]	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support [2]	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA [3]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security [4]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot						
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts						
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates [5])	28K Logic Cells (~430K)	74K Logic Cells (~1.1M)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	275K Logic Cells (~4.1M)	350K Logic Cells (~5.2M)	444K Logic Cells (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Extensible Block RAM (# 36 Kb Blocks)	240 KB (60)	380 KB (95)	560 KB (140)	1,060 KB (265)	2,000 KB (500)	2,180 KB (545)	3,020 KB (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACS	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)	—	Gen2 x4	—	Gen2 x8	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC [6]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security [4]	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration						
Speed Grades	Commercial (0°C to 85°C)	-1			-1			N/A
	Extended (0°C to 100°C)	-2, -3			-2, -3			N/A
	Industrial (–40°C to 100°C)	-1, -1L, -2			-1, -2, -2L			

	Package [7][8]	CLG225 [9]	CLG400	CLG485 [7]	CLG400	CLG484	SBG485 [7] SBV485	FBG484 FBV484	FBG676 FBV676	FFG676 FFV676	FBG676 FBV676	FFG676 FFV676	FFG900 FFV900	FBG676 FBV676	FFG676 FFV676	FFG900 FFV900	FFG900 FFV900	FFG1156 FFV1156
Packages	Size (mm)	13x13	17x17	19x19	17x17	19x19	19x19	23x23	27x27	27x27	27x27	27x27	31x31	27x27	27x27	31x31	31x31	35x35
	Pitch (mm)	0.8	0.8	0.8	0.8	0.8	0.8	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
	Processing System User I/Os (excludes DDR dedicated I/Os) [8]	32	54	54	54	54	54	54	54	54	54	54	54	54	54	54	54	54
	Multi-Standards and Multi-Voltage SelectIO™ Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)	54	100	150	125	200	50	100	100	100	100	100	212	100	100	212	212	250
	Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)	—	—	—	—	—	100	63	150	150	150	150	150	150	150	150	150	150
	Serial Transceivers	—	—	4	—	—	4	4	4	4	8	8	16	8	8	16	16	16
	Maximum Transceiver Speed (Speed Grade Dependent)	N/A	N/A	6.25 Gb/s	N/A	N/A	6.6 Gb/s	6.6 Gb/s	6.6 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s	6.6 Gb/s	12.5 Gb/s	12.5 Gb/s	10.3125 Gb/s	10.3125 Gb/s

ds187(v1.11)

Notes: 1. 1 GHz processor frequency is available only for -3 speedgrades for devices in flip-chip packages. Please see the data sheet for more details.
2. Z-7010 in CLG225 has restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
5. Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.

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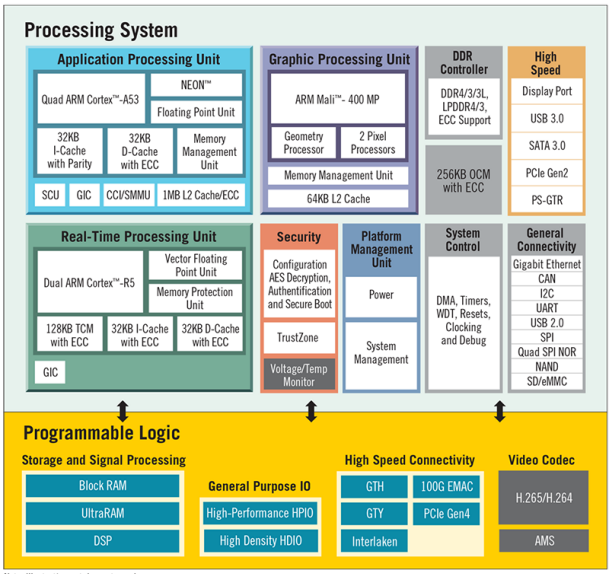
Zynq UltraScale+ MPSoC



Note: Illustration not drawn to scale.

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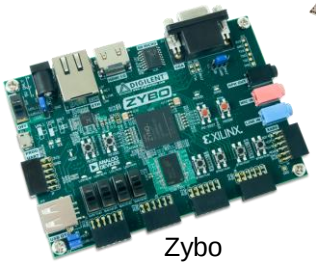
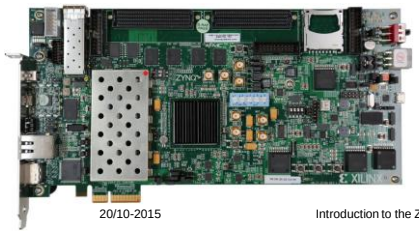
Zynq boards

Mini-ITX

MicroZed



Zybo



Zc706

Zynq MMP

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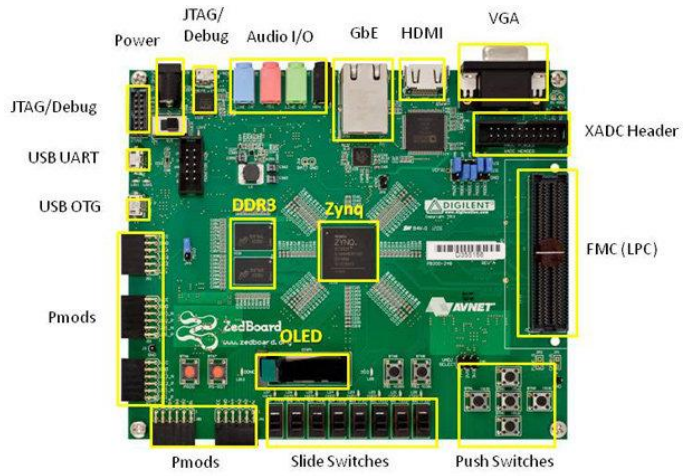
Zynq boards - Zedboard



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Second hour – AXI interface

- Overview
- Axi4-stream
- Axi4-lite
- Axi4

Overview – Axi4

- Defined in the AMBA 3 specification from ARM
- Targeted at high performance, high clock frequency systems
- Has a lot of features useful for SOCs:
  - Separate address/control and data phases
  - Support for unaligned data transfers
  - Burst based transactions with interface logic
  - Supports atomic operations, QoS and memory coherency features.

Types

- Three types:
  - **Axi4-stream**
    - Supports single or multiple streams on same wires
    - Supports multiple data widths within same interconnect
  - Axi4-lite
    - Transaction length of one
    - All data accesses are same size as bus width
    - 32/64 bit data widths
    - No exclusive access
  - Axi4
    - Supports burst length up to 256 beats
    - Supports different sized data accesses
    - Support for exclusive access
    - Includes Quality of service signalling

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Axi4-stream

- Only contains a data channel:
  - Typically *Ready*, *Valid*, *Data*, *Last* (+ *clk*)
- May or may not contain packets
  - Master and slave need knowledge on format

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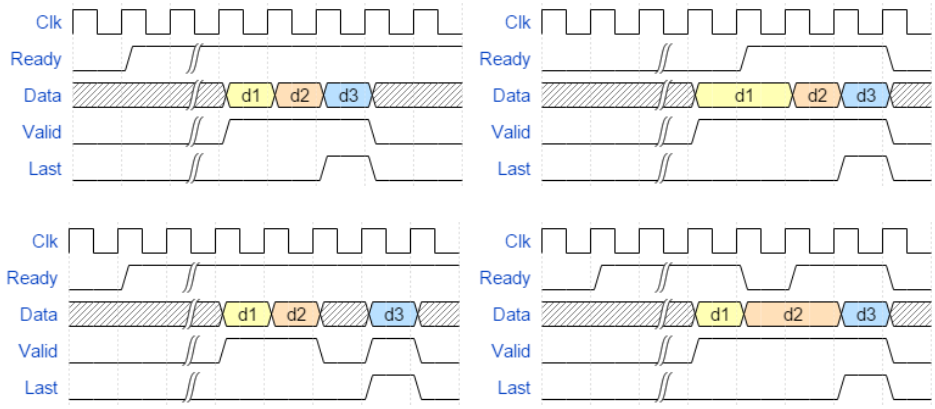
Axi4-stream examples



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    - Includes Quality of service signalling

Axi4-lite

- Two independent channels: Read and Write
- Response is always generated

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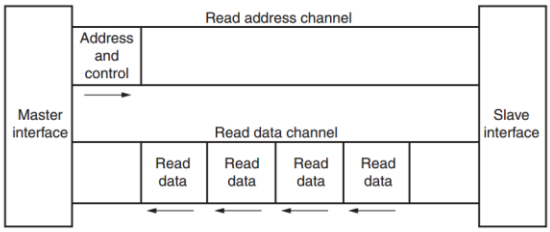
Axi - reading



	Axi4-lite
Glbl	ACLK
	ARESETN

	Axi4-lite
AR	ARReady
	ARAddr
	ARValid
	ARProt
	ARCache

	Axi4-lite
R	RReady
	RData
	RValid
	RResp

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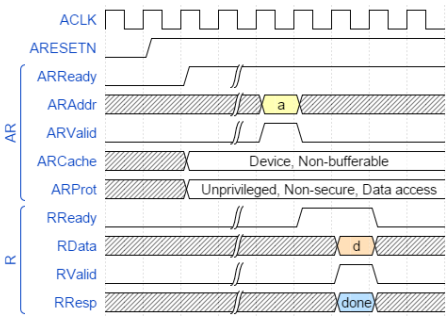
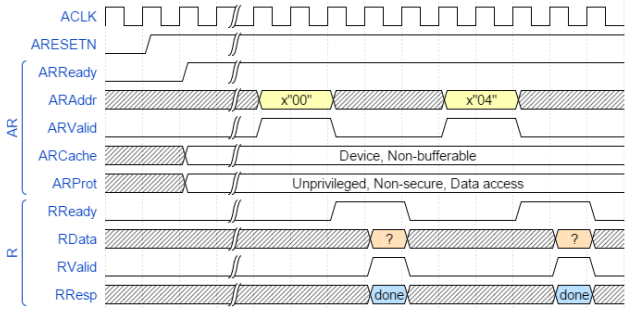
Axi4-lite Read examples





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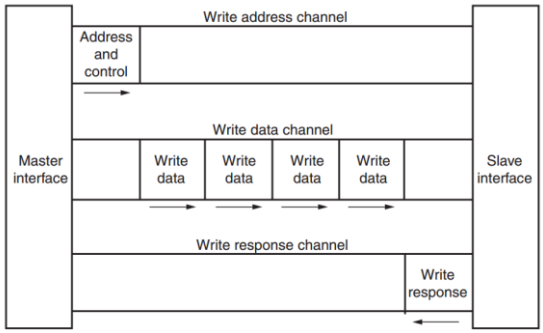
Axi - writing



	Axi4-lite
Glbl	ACLK
	ARESETN

	Axi4-lite
AW	AWAddr
	AWCache
	AWValid
	AWReady

	Axi4-lite
W	WData
	WStrb
	WValid
	WReady

	Axi4-lite
B	BResp
	BValid
	BReady

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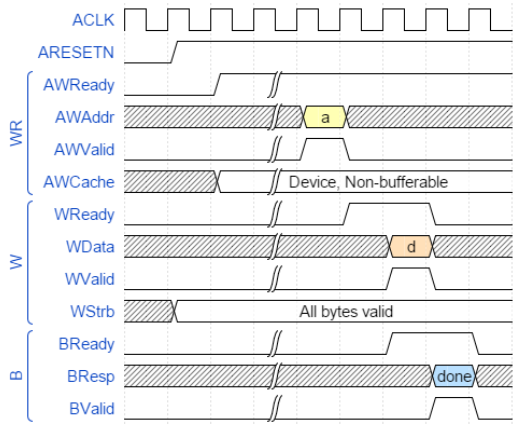
Axi4-lite
Write example



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    - No exclusive access
  - **Axi4**
    - Supports burst length up to 256 beats
    - Supports different sized data accesses
    - Support for exclusive access
    - Includes Quality of service signalling

Axi4

- Like AXI4-lite, but with additional features
  - Bursts of up to 256 beats
  - Exclusive access
  - Memory management / coherency
  - Quality of service
- Can be translated into AXI4-lite by AXI interconnects

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Axi4 - reading

	Axi4
AR	ARId
	ARReady
	ARAddr
	ARValid
	ARLen
	ARSize
	ARBurst
	ARLock
	ARCache
	ArProt
	ARQos
	ARRegion
	ARUser

	Axi4
R	Rid
	RReady
	RData
	RValid
	RResp
	RLast
	RUser

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Axi4 - writing

	Axi4
AW	AWId
	AWReady
	AWAddr
	AWValid
	AWLen
	AWSize
	AWBurst
	AWLock
	AWCache
	AWProt
	AWQos
	AWRegion
	AWUser

	Axi4
W	WId
	WReady
	WData
	WStrb
	WValid
	WLast
	WUser

	Axi4
B	BId
	BResp
	BUser
	BValid
	BReady

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Second hour – AXI interface

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