Nyquist Rate D/A Converters (12.1-12.4)

Tuesday 2nd of March, 2010, 9:15-11:00

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Last time – and today, Tuesday 2nd of March:

Last time:

10.3 First-order filters
10.4 Biquad filters (high-Q)
10.5 Charge injection
10.7 Correlated double sampling techniques
11.1 Ideal D/A converter
11.2 Ideal A/D converter
11.3 Quantization noise
11.4 Signed codes

Today:

11.5 Performance Limitations
12.1 Decoder-based converters
12.2 Binary-scaled converters
12.3 Thermometer-code converters
12.4 Hybrid converters

10:55: 5 minute survey by ”Micro”
Offset and gain error

- In a D/A converter ("DAC") the offset error is defined to be the output that occurs for the input code that should provide zero output. For an A/D converter ("ADC") the offset error is the deviation of $V_{0...01}$ from $\frac{1}{2}$ LSB.

- The gain error is the difference at the full scale value between ideal and actual curves when the offset has been reduced to zero. For a DAC it is given in units of LSBs.

**ADC:**

\[
E_{\text{gain(A/D)}} = \left( \frac{V_{0...1}}{V_{\text{LSB}}} - \frac{V_{0...01}}{V_{\text{LSB}}} \right) - (2^N - 2)
\]  

(11.25)
After both offset and gain errors have been removed, the integral nonlinearity (INL) error is defined to be the deviation from a straight line. Possible straight lines: endpoints of the converters transfer response, best-fit straight line such that the difference (or mean squared error) is minimized.
Differential nonlinearity error (DNL)

- Ideally, each analog step size is equal to 1 LSB. **DNL** is variation in step size from $V_{\text{LSB}}$ (after removal of gain and offset errors). Ideally DNL is 0 for all digital values. DNL is in “J & M” defined for each digital word, whereas other sometimes refer to DNL as the maximum magnitude of DNL values.
Monotonicity in DACs

• A monotonic DAC is one in which the output always increases as the input increases (slope of the transfer response is of only one sign.)

• If the maximum DNL error is less than 1 LSB, the DAC is guaranteed to be monotonic.

• However, many monotonic converters may have a maximum DNL greater than 1 LSB.

• Similarly, a converter is guaranteed to be monotonic if maximum DNL is < 1 LSB.

• 3-bit nonmonotonic example in the figure is from Analog-Digital conversion handbook by Analog Devices
D/A (DAC) settling time and sampling rate

• In a DAC the **settling time** is defined as the time it takes for the converter to settle within some specified amount of the final value (usually 0.5 LSB).

• The **sampling rate** is the rate at which samples can be continuously converted and is typically the inverse of the settling time.

• Different combinations of input vectors give different settling times.

**Fig 3.9** Risetime 6 bit DAC, input 0 to 128. (Xdivision = 50ns)
Nyquist Rate D/A Converters

• 12.1 Decoder-based converters
  resistor string conv.
  folded resistor string conv.
  multiple R-string converters

• 12.2 Binary-Scaled converters
  binary-weighted resistor converters
  reduced resistance-ratio ladders
  R-2R-based converters
  charge-redistribution switched-capacitor conv.
  current-mode conv.

• 12.3 Thermometer-code converters
  thermometer-code current-mode D/A converters
  single-supply positive-output converters
  dynamically matched current sources

• 12.4 Hybrid converters
  resistor-capacitor hybrid converters
  segmented converters
Some systems exploiting data converters, "Allen & Holberg"

---

**Figure 10.1-1** (a) A/D converters and (b) D/A converters in signal processing systems.
Ideal D/A converter

\[ B_{in} = b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N} \]

\[ V_{out} = V_{ref}(b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N}) \]
Ideal D/A converter

\[ V_{\text{LSB}} = \frac{V_{\text{ref}}}{2^N} \]

1 LSB = \( \frac{1}{2^N} \)

2-bit DAC

\[ \frac{V_{\text{LSB}}}{V_{\text{ref}}} = \frac{1}{4} = 1 \text{ LSB} \]
12.1 Decoder-Based Converters

- Creates $2^N$ reference signals and passes the appropriate signal to the output, depending on the digital input word.
- The switching network produces one, and only one, low impedance path between the resistor string and the input of the buffer.
- Relatively compact switches if n-channel devices are used instead of transmission gates.
Resistor String Converters (12.1)

- Only one path between resistor string and D/A-output
- Guaranteed monotonicity, provided that the voltage follower does not have too large offset
- Compact design when using only n-transistors (no contacts)
- Polysilicon resistors may give resolution up to 10 bit
- Delay through switch network is the major speed limitation of the circuit
- \(2^N\) resistors are required (when only one resistor string is included)
Resistor String Converters (12.1)

- High-speed implementation (when compared to the previous one), due to maximum of one switch in series
  - Less resistance through switches
  - The switches are controlled by digital logic
  - More area for the decoder compared to the previous DAC
  - Larger capacitance on the buffer input, due to the $2^N$ transistors connected to it
  - Pipelining may be applied for “moderate speed”
  - $2^N$ resistors are required
Estimating the time constant for n resistors and capacitors in series (ex. 12.2)

\[ \tau = RC + 2RC + \ldots + nRC = RC \left( 1 + 2 + \ldots + n \right) \]

\[ \tau = RC \cdot \frac{n(n+1)}{2} \]

\[ \begin{array}{c|cccc}
   n & 1 & 5 & 10 & 50 & 100 \\
   \frac{(n+1)n}{2} & 1 & 15 & 55 & 225 & 5050 \\
   \frac{n^2}{2} & 1 & 2.5 & 5 & 25 & 1250 \\
\end{array} \]

\[ V_{out} \approx (1 - e^{-\frac{\tau}{RC}}) V_P \]

\[ V_{out} = 0.999 \times V_P \text{ : about } 7.2 \tau \text{ is needed} \]
Folded Resistor-String Converters 12.1

- Reducing size of digital circuitry and capacitive loading
- $2^N$ resistors are required
- $b_1b_2$: Most significant bits in the 4 bit case (selects one single word line.)
- Structure similar to what can be found in digital memories.
- OBS! NMOS switches here
- Number of transistor junctions connected to the output line is now $2 \sqrt{2^N}$, instead of $2^N$
- 4 bit case: 8 instead of 16
- 8 bit case: 32 instead of 256
- 10 bit case: 64 instead of 1024
- When a word line goes high, all the bit lines must be pulled to new levels, limiting speed (no increase equal to the ratio ($\frac{2 \sqrt{2^N}}{2^N}$))
Multiple R-String Converters (12.1)

• A second tapped resistor string is connected between buffers whose inputs are two adjacent nodes of the first resistor string, as shown.

• In this 6-bit case the 3 MSBs determine the two adjacent nodes. The 2nd ("fine") string linearly interpolates between the two adjacent voltages from the first ("coarse") resistor string.

• Additional logic needed to handle polarity switching, related to which intermediate buffer has the highest voltage on the input.

• Guaranteed monotonicity assuming matched opamps and voltage insensitive offset voltages.

• $2 \times 2^{N/2}$ resistors are required.

• Relaxed matching requirements for the 2nd resistor string.

• Ex.: 10 bit, 4 bits for the 1st string, matched to 0.1 %. Requirements for 2nd string? $2^4 \times 0.1 \% = 1.6 \%$
12.2 Binary-Scaled Converters

- Combining a set of signals that are related in a binary fashion
- Typically currents (resistors or plain current) or binary weighted arrays of charges
- Example: 4-bit binary-weighted resistor DAC:

![4-bit circuit diagram]

- Circuit diagram of a 4-bit binary-weighted resistor DAC, with resistors labeled 2R, 4R, 8R, and 16R, and an operational amplifier.
Binary-Weighted Resistor Converters (12.2)

\[ V_{out} = -R_F V_{ref} \left( -\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \cdots \right) \]

- Few switches and resistors
- Large resistor and current ratios \((2^N)\)
- Monotonicity not guaranteed
- Prone to glitches for high-speed operation
Glitches – from Analog Digital Conversion Handbook

Glitch Impulse Area

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both (see Figure 2.94). This uncontrolled movement of the DAC output during a transition is known as a glitch. It can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC operating more quickly than others and producing temporary spurious outputs.

*Figure 2.94: DAC Transitions (Showing Glitch)*

Capacitive coupling frequently produces roughly equal positive and negative spikes (sometimes called a *doublet glitch*) which more or less cancel in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger and of greater concern.
Glitches waste energy and produce noise

- Glitches can be seen as unwanted transitions on the output, instead of a monotonous move from one output value to the next.
- Mainly the result of different delays occurring when switching different signals.

Potential cures:
- Exact matching in time (difficult)
- Reducing the bandwidth by placing $C$ across $R_f$ in a circuit similar to the one in fig. 12.13.
- Add S/H to the output.
- Modify some or all of the digital word from binary to thermometer code (most popular).

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<tr>
<td>7</td>
<td>111</td>
<td>1111111</td>
</tr>
</tbody>
</table>
Reduced-Resistance-Ratio Ladders (12.2)

- Reducing the large resistor ratios (compared to Fig. 12.7, left) in a binary weighted array by introducing a series resistor (right).
- Same relationship to the digital binary signals as in the previous case, but with one-fourth the resistance ratio (4/2 - not 16/2)

Somewhat similar to the R-2R ladder structure..
R-2R ladder

\[ R_{4} = 2R \]

\[ R_{4} = \frac{2R \cdot 2R}{2R + 2R} = \frac{4R^2}{4R} = R \]

\[ R_{2} = R + R_{4} = R + R = 2R \]

\[ R_{2} = \frac{2R \parallel R_{2}'}{2R} = \frac{2R \cdot 2R}{4R} = R \]

\[ R_{1} = R + R_{3} = R + R = 2R \]

\[ R_{1} = 2R \parallel R_{1}' = R \]

\[ R_{i} = R + R_{i} = R \]

\[ R_{i} = 2R \parallel R_{i}' = R \]

\[ R_{i}' = 2R \quad \text{for all } i \]
R-2R-Based Converters (12.2)

- Only two resistor values
- Improved matching
- $\rightarrow$ smaller size and better accuracy

\[ R'_4 = 2R \]
\[ R_4 = 2R \parallel 2R = R \]
\[ R'_3 = R + R_4 = 2R \]
\[ R_3 = 2R \parallel R'_3 = R \]
4-bit R-2R Resistor Ladder (12.2)

- The current is scaled by controlling the switches
- Important to scale the switches accordingly
  - Ensuring equal voltage drop across the switches
- Suited for fast operation
  - $V_{out}$ is the only changing voltage
R-2R Resistor Ladder with equal current through all switches

(12.2)

- Not necessary to scale switch sizes (Equal current)
- Slower due to changing node voltages
• Current-mode DACs are very similar to resistor-based converters, but intended for higher speed applications
• The output current is converted to a voltage through the use of $R_F$
Binary weighted current mode DAC (12.2)(fig. 12.13)

Fig. 12.13 Binary weighted current mode DACs are often used as digital-to-analog converters, but in some applications, but current is controlled through the use of $R_F$. 

$V_{out}$
Parallel charge sharing DAC principle

**PARALLEL CHARGE SCALING DAC**

DAC operation based on capacitive voltage division

\[ V_{out} = \frac{C_x}{C_x + C_y + C} \cdot V_{ref} \]

Make \( C_x \) and \( C_y \) function of incoming DAC digital word

Example: 4-bit DAC, Charge Sharing

Reset phase:

\[ V_{ref} \]

Charge phase:

Input code 1110:

\[ V_{out} = \frac{2^3 C + 2^2 C + 2^1 C}{2^4 C} \cdot V_{ref} = \frac{(2+4+8)}{16} \cdot V_{ref} \]
Capacitance ratios defining voltage gain

SWITCHED CAPACITOR GAIN STAGES

One of the most common functions in analog signal processing is voltage amplification, as shown.

The input-output relation:

\[
\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1}
\]

If \( Z_2 = k \cdot Z_1 \), where \( k \) is a constant, a (fixed) gain is achieved.

By switching in different \( C \), the voltage gain may change, depending on the input.
Charge-Redistribution Switched Capacitor Converter (12.2) (fig. 12.12)

- By replacing the input capacitor of an SC gain amplifier by a programmable capacitor array (PCA) a charge based converter is obtained.
- Employs correlated double sampling (CDS) – insensitive to 1/f noise, input-offset voltage and finite amplifier gain.
- An additional sign bit may be realized by interchanging the clock phases.
- Carefully generated clock waveforms and a deglitching capacitor are required.
- Digital codes must change only when the input-side of the capacitors are connected to ground.
Thermometer-Code Converters (Chapter 12.3) - number of 1s represents the decimal value

• + compared to binary counterpart:
• Lower DNL errors
• Reduced glitching noise
• Guaranteed monotonicity
• - compared to binary counterp.:
• Need $2^N - 1$ digital inputs to represent $2^N$ input values

<table>
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<tr>
<th>decimal</th>
<th>Binary b1b2b3</th>
<th>Thermometer code d1d2d3d4d5d6d7</th>
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<tr>
<td>7</td>
<td>111</td>
<td>1111111</td>
</tr>
</tbody>
</table>
Thermometer Based 3-bit DAC (12.3)

- Equal resistor sizes
- Equal switch sizes
- $2^N$ resistors required
Thermometer-Code Charge-Redistribution DAC (12.3) (Fig. 12.16)

- $2^N$ capacitors required

Top Capacitors are Connected to Ground

Bottom Capacitors are Connected to $V_{ref}$
Thermometer-code Current-Mode D/A-Converter (12.3)

- Thermometer-code decoder in both row and column, for inherent monotonicity and good DNL
- Current is switched to the output when both row and column lines for a cell are high
- Cascode current source used for improved current matching
- Suited for high speed, with output fed directly into a resistor (50 or 75 Ohms), instead of an output opamp.
- The delay to all switches must be equal (suppress glitching)
- Important that the edges of \( d_i \) and \( d'_i \) are synchronized
Thermometer-code Current-Mode DAC - example

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

• Cascode current sources
• Latches connected to decoding
• One gate in the differential pair may be put to a dc level, to improve speed.

![Diagram of the DAC](image)

**Fig. 2.** Two-step decoding.

**Fig. 3.** High-speed decoding circuit.

**Fig. 4.** Circuit diagram of the LSB current source.

**Fig. 5.** Configuration of current source: (a) Single-transistor configuration, (b) Cascode configuration.

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>CHARACTERISTICS OF THE DAC</th>
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<tbody>
<tr>
<td>Resolution</td>
<td>8 bit</td>
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<td>Settling Time</td>
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<tr>
<td>Rise/Fall Time</td>
<td>5.5 ns</td>
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<td>Integral Linearity Error (DC)</td>
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<tr>
<td>Differential Linearity Error (DC)</td>
<td>0.22 LSB (Typ.)</td>
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<td>Glitch Energy</td>
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<td>Power Consumption</td>
<td>145 mW</td>
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<tr>
<td>Chip Size</td>
<td>9.65 mm x 2.35 mm</td>
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</table>
For **fast** single-supply positive-output

**One side of each current-steering pair connected to** \( V_{\text{bias}} \), **rather than the inversion of the bit signal**, to maintain current matching. When the current is steered to the output through \( Q_2 \), the drain-source voltage across the current source, \( Q_3 \), remains mostly constant if \( V_{\text{out}} \) stays close to zero, such that \( Q_2 \) remains in the active region.

Thus, \( Q_2 \) and \( Q_3 \) effectively form a **cascode current source** when driving current to the output.

Does not need \( d_1 \) and \( d_1' \); reduces complexity and **removes the need for precisely timed edges** to avoid glitches.
Dynamically Matched Current Sources
(12.3)
- for high resolution

A Low-Power Stereo 16-bit CMOS D/A Converter for Digital Audio

HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, D. WOUTER J. GROENEVELD, AND HENDRICK A. H. TERMEER

- Current sources are periodically being regulated to ideally the same value (matched) during normal operation, to ensure proper resolution.

- A “once and for all” matching of each current source is not enough due to mechanisms including temperature drift and gate leakage.
Dynamically Matched Current Sources

(12.3)

- 6 MSB realized using a thermometer code. (binary array for the remaining bits)
- All currents are matched against $I_{ref}$, one after one, to get the same precise value on all $I_{di}$.
- One extra current source is included to provide continuous operation, even when one of the sources is being calibrated.
Dynamic matched current sources – method for calibration

- $I_{di}$ is connected to $I_{ref}$ during calibration. This places whatever voltage is necessary across the parasitic $C_{gs}$ so that $I_{di}$ equals $I_{ref}$. When $S_i$ is opened $I_{di}$ remains nearly equal to $I_{ref}$.

- Major limitation in matching the 64 current sources is due to differences in clock feedthrough and charge injection of the switches $S_i$. → have relatively large $C_{gs}$ and $V_{gs}$ (large $V_{gs}$ so that a certain voltage difference will cause a smaller current deviation.)

- Using $0.9I_{ref}$ in parallell makes $Q_1$ need only to source a current near $0.1I_{ref}$. With such an arrangement a large low-transconductance device can be used (ex.: $W/L=1/8$)

![Diagram](image.png)
12.4 Hybrid Converters

- Combination of different techniques, like for example decoder based, binary scaled, and thermometer-code converters
- Hybrid converters combine the advantages of different approaches for better performance
- **Example:** Thermometer code used for MSBs, while using a binary-scaled technique for the lower LSBs to reduce glitching. Using binary scaled for the LSBs, where glitching requirements are reduced, may save valuable chip area.
Resistor-Capacitor Hybrid Converters (12.4)

- Top 7 MSBs determine which pair of voltages across a single resistor is passed on to the 8-bit capacitor array.
- A 7-bit resistor-string DAC is combined with an 8-bit SC binary-weighted DAC for a 15-bit converter.
- 15-bit monotonicity, without trimming.

Fig. 12.21 One example of a 15-bit resistor-capacitor hybrid D/A converter.

High-Resolution Low-Power CMOS D/A Converter

JOHN W. YANG AND KENNETH W. MARTIN, SENIOR MEMBER, IEEE

Abstract — A very low-power, high-resolution, medium-speed D/A converter is described. The converter was realized using a standard analog CMOS technology. It achieved 15-bit monotonicity and less than 0.07-percent overall linearity at a clock frequency of 100 kHz, without requiring any trimming or calibration. The measured SNR was 85 dB, the power dissipation was less than 10 mW, and the distortion for a sinusoidal output was less than 0.04 percent. The D/A converter is intended for battery-powered speech and music synthesis applications where high dynamic range, low power, and low cost are all important.
Segmented Converters (12.4)

- Combination of thermometer- and binary
- 2 MSB’s are thermometer (reduces glitches)
- 4 LSB’s are binary
- High bits switched to the output, low bits to ground
## A few published DACs

<table>
<thead>
<tr>
<th>Publication year</th>
<th>SFDR @Nyquist [dB]</th>
<th>ENOB @ Nyquist</th>
<th>Nyquist update rate, [Ms/s]</th>
<th>Power consumpt. [mW]</th>
<th>Area [mm²]</th>
<th>Supply voltage [V]</th>
<th>Technology [nm]</th>
<th>other</th>
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<td>2009</td>
<td>&gt;60dB</td>
<td>9.7</td>
<td>1000</td>
<td>188</td>
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<td>65</td>
<td>Current steering</td>
<td>Lin et al., ISSCC '09</td>
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<td>2008</td>
<td>80</td>
<td>12.9</td>
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<td>119</td>
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<td>59</td>
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<td>56</td>
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*Note: ENOB stands for Effective Number of Bits.*
Next Tuesday (9/3-08):

- Chapter 13 Nyquist Analog-to-Digital Converters
Additional literature

• Lecture Notes, University of California, Berkeley, EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/