Nyquist Rate Analog-to-Digital Converters

Tuesday 9th of March, 2009, 9:15 – 11:00

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Last time – and today, Tuesday 9th of March:

Last time:
12.1 Decoder-Based Converters
12.2 Binary-Scaled Converters
12.3 Thermometer-Code Converters
12.4 Hybrid Converters

Today – from the following chapters:
13.1 Integrating Converters
13.2 Successive-Approx. Converters
13.3 Algorithmic (or cyclic) A/D Converters
13.4 Flash (or parallel) converters
13.5 Two-Step A/D converters
13.6 Interpolating A/D Converters (16/3-10)
13.7 Folding A/D Converters (16/3-10)
13.8 Pipelined A/D Converters
13.9 Time-Interleaved A/D Converters
## Different A/D Converter Architectures

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Different ADCs depending on needs

Figure 1. ADC architectures, applications, resolution, and sampling rates.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]
A/D-conversion – Basic Principle

\[ V_{\text{ref}}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{\text{in}} \pm x \]

where \( \frac{1}{2} \text{V}_{\text{LSB}} < x < \frac{1}{2} \text{V}_{\text{LSB}} \)

- The analog input value is mapped to discrete digital output value
  - Quantization error is introduced
Integrating Converters (13.1)

- \( V_x(t) = V_{in} \frac{t}{RC} \) (\( V_x \) ramp derivative depending on \( V_{in} \))
- High linearity and low offset/gain error
- Small amount of circuitry
- Low conversion speed
  - \( 2^{N+1} \times \frac{1}{T_{clk}} \) (Worst case)

(Vin is held constant during conversion.)
Integrating Converters

- The digital output is given by the count at the end of $T_2$
- The digital output value is independent of the time-constant RC
Dual slope ADC

Positive integrator used in dual-slope ADCs

\[ U_{\text{out}} = \frac{1}{RC} \int_0^t U_{\text{in}} \, dt \]

\[ = \frac{V_{\text{in}}}{RC} t \]

Example: 16-bit two-slope ADC with \( V_{\text{in}} = 3V \), \( V_{\text{max}} = 4V \) and \( T_1 = 20\,\text{ms} \). RC - constant? Clock freq:

\[ f_{\text{clk}} = \frac{1}{T_{\text{clk}}} = \frac{2\,\text{ms}}{20\,\text{ms}} \approx 3.28\,\text{MHz} \]

Equation (13.15):

\[ V_x = \frac{V_{\text{in}} T_1}{RC} = \frac{4V \cdot 3V \cdot 20\,\text{ms}}{RC} \]

\[ \uparrow \]

\[ RC = 15\,\text{ms} \]
Integrating Converters – careful choice of T1 can attenuate frequency components superimposed on the input signal.

-20 dB/decade slope

|H(f)|
(dB)

-30
-20
-10
0

Frequency (Hz) (Log scale)

- In the above case, 60 Hz and harmonics are attenuated when T1 is an integer multiple of 1/60 Hz.
- Sinc-response with rejection of frequencies multiples of 1/T₁
Successive approx ADC algorithm

(13.2)

- If we have weights of 1 kg, 2 kg, 4 kg, 8 kg, 16 kg, 32 kg and will find the weight of an unknown X assumed to be 45 kg.

\[ \begin{aligned}
\text{TEST} & \quad \text{ASSUME } X = 45 \\
\text{IS } X \geq 32? & \quad \text{YES } \rightarrow \text{RETAIND } 32 \rightarrow 1 \\
\text{IS } X \geq (32 + 16)? & \quad \text{NO } \rightarrow \text{REJECT } 16 \rightarrow 0 \\
\text{IS } X \geq (32 + 8)? & \quad \text{YES } \rightarrow \text{RETAIND } 8 \rightarrow 1 \\
\text{IS } X \geq (32 + 8 + 4)? & \quad \text{YES } \rightarrow \text{RETAIND } 4 \rightarrow 1 \\
\text{IS } X \geq (32 + 8 + 4 + 2)? & \quad \text{NO } \rightarrow \text{REJECT } 2 \rightarrow 0 \\
\text{IS } X \geq (32 + 8 + 4 + 2 + 1)? & \quad \text{YES } \rightarrow \text{RETAIND } 1 \rightarrow 1 \\
\end{aligned} \]

TOTALS: \[ X = 32 + 8 + 4 + 1 = 45_{10} = 101101_2 \]

\[ 1*32 + 0*16 + 1*8 + 1*4 + 0*2 + 1*1 = 45_{10} \]

Figure 4. Successive-approximation ADC algorithm using balance scale and binary weights.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]
Successive-Approximation Converters

- Uses **binary-search** algorithm
- Accuracy of $2^N$ requires $N$ steps
- The digital signal accuracy is within +/- 0.5 $V_{\text{ref}}$
- Medium speed
- Medium resolution
- Relatively moderate complexity
 DAC-Based Successive Approximation

- \( V_{\text{in}} \) is adjusted until the value is within 1LSB of \( V_{\text{in}} \)
- Starts with MSB and continues until LSB is found
- Requires DAC, S/H, Comparator and digital logic
- The DAC is typically limiting the resolution
Succ. Approx ADC, example 13.2

Example 13.2

\[ V_{ref} = 8 \text{V} \]
\[ V_{in} = 2.831 \text{V} \]

3-bit conversion

- **cycle 1**: \( B_{out} = 100 \), so that \( V_{D/A} = 4.0 \text{V} \). Since \( V_{in} < V_{D/A} \), \( b_1 \rightarrow 0 \)
- **cycle 2**: \( B_{out} = 010 \), so that \( V_{D/A} = 2.0 \text{V} \). Since \( V_{in} > V_{D/A} \), \( b_2 \rightarrow 1 \)
- **cycle 3**: \( B_{out} = 011 \), \( b_3 \rightarrow 1 \) \( V_{in} = 3.0 \text{V} \). Since \( V_{in} < V_{D/A} \), \( b_3 \rightarrow 0 \)

010
Sample $V_{in}$, $\bar{c} = 0$

$V_{p/A} = \frac{V_{ref}}{2^{\bar{c}+1}}$

$V_{in} > V_{p/A}$

- $b_{\bar{c}+1} = 1$
- $\bar{c} \rightarrow \bar{c} + 1$
- $V_{0/A} \rightarrow V_{0/A} + \frac{V_{ref}}{2^{\bar{c}+1}}$

$V_{in} > V_{p/A}$

- $b_{\bar{c}+1} = 0$
- $\bar{c} \rightarrow \bar{c} + 1$
- $V_{PA} \rightarrow V_{p/A} - \frac{V_{ref}}{2^{\bar{c}+1}}$

Ex. 13.2

$V_{\text{ref}} = 8V$, $V_{in} = 2.831V$

$V_{p/A} = \frac{V_{\text{ref}}}{2^{\bar{c}+1}} = \frac{8V}{2^1} = 4V$

$V_{in} > V_{p/A} \Rightarrow 2.831V > 4V \Rightarrow \text{NO}$

$b_{\bar{c}+1} = b_{\bar{c}+1} = b_1 = 0$

$\bar{c} \rightarrow \bar{c} + 1 = 0 + 1 = 1$

$V_{P/A} \rightarrow 4V - \frac{8}{2^2} = 4V - 2V = 2V$

$\bar{c} = 1 \geq 3 \Rightarrow \text{NO}$

$V_{in} > V_{p/A} \Rightarrow 2.831V > 2V \Rightarrow \text{YES}$

$b_{\bar{c}+1} = b_{\bar{c}+1} = 1 \Rightarrow b_2 = 1$

$\bar{c} \rightarrow \bar{c} + 1 = 1 + 1 = 2$

$V_{p/A} \rightarrow V_{p/A} + \frac{V_{\text{ref}}}{2^{\bar{c}+1}} = 2V + \frac{8}{2^2} = 2V + 2V = 3V$

$\bar{c} = 2$, $2 \geq 3 \Rightarrow \text{NO}$

$V_{in} > V_{p/A} \Rightarrow 2.831V > 3V \Rightarrow \text{NO}$

$b_3 = 0$

$\bar{c} \rightarrow 2 + 1$

$V_{p/A}$ updated, $3 \geq 7 \Rightarrow \text{STOP}$
Charge-Redistribution A/D-Converter (unipolar)

- Instead of using a separate DAC and setting it equal to the input voltage (within 1 LSB) as for the DAC based converter from figure 13.5, one can use the error signal equaling the difference between the input signal, $V_{in}$, and the DAC output, $V_{D/A}$. 

Fig. 13.6 Flow graph for a modified successive approximation (divided remainder).
Numbers from 13.2 setting an error signal $V$ equal to $V_{in} - V_{D/A}$ – modified succ. approx as in fig. 13.6

Example 13.2: Using modified succ. approx (divided remainder)

Error signal $V = V_{in} - V_{DAC}$

$V = +2.831V \div 4V = -1.169V$

-1.169 > 0? NO, $b_1 = 0$

$V = -1.169V + 0.831V = 0.831V$

$\ell = \ell + 1 = 2$

$\ell = 2 > 3$? NO

$0.831V > 0$?

YES

$b_2 = 1$

$V = (0.831 - 0.169)V = -0.169V$

$\ell = \ell + 1 = 3$

$\ell > 3$?

NO

$-0.169V > 0$?

NO $\Rightarrow b_3 = 0$

$b_1b_2b_3 = 010$

(liner in ex. 13.2)
Unipolar Charge-Redistribution A/D-Converter

1. Sample mode

\[ V_x \approx 0 \]

2. Hold mode

\[ V_x = -V_{in} \]

3. Bit cycling

\[ V_x = -V_{in} + \frac{V_{ref}}{2} \]
Charge-Redistribution A/D-Converter

- Sample mode:
  - All capacitors charged to Vin while the comparator is reset to its threshold voltage through S₂. The capacitor array is performing S/H operation.

- Hold mode:
  - The comparator is taken out of reset by opening S₂, then all capacitors are switched to ground. Vₓ is now equal to –Vin. Finally S₁ is switched so that V_ref can be applied to the capacitors during bit-cycling.

- Bit-cycling:
  - The largest capacitor is switched to V_ref. Vₓ goes to –Vin + V_ref/2. If Vₓ is negative, then V_in is greater than V_ref/2 and the MSB capacitor is left connected to V_ref. Otherwise the MSB capacitor is disconnected and the same procedure is repeated N times.
EX. 13.3 p. 497

Find intermediate node voltages at $V_x$ during the operation of the 5-bit charge-redistribution converter shown in Fig. 13.7. Assume $\frac{8C}{3}$ as a parasitic cap at $V_x$.

SAMPLE MODE:

\[
V_{in} \xrightarrow{S_0 \rightarrow S_1} \frac{2C}{32 + 8} (-V_{in}) \xrightarrow{S_0 \rightarrow S_1} V_x = 0
\]

\[
V_x = \frac{32}{40} \cdot (-1.23 \text{ V}) = -0.984 \text{ V}
\]

HOLD MODE:

\[
V_x = \frac{32}{32 + 8} \cdot (-V_{in}) \xrightarrow{S_0 \rightarrow S_1} \frac{10C}{3C_1 + C_2} \xrightarrow{S_0 \rightarrow S_1} V_{out} = \frac{C_x}{C_x + C_Y} \cdot V_{ref}
\]

\[
V_{ref} \xrightarrow{S_0 \rightarrow S_1} \frac{C_1}{C_2}
\]

$C_x$ and $C_Y$ functions of digital word switching

1) Sample mode
2) Hold mode
3) Bit cycling
\[ V_{\text{ref}} = 5V \]

**Bit Cycling**

- \( b_1 \) is switched controlling the 16C capacitor:
  \[ V_x = -0.984V + \frac{16}{82+6} \cdot 0.5V \]
  \[ = -0.984V + 2V = 1.016V \]
  \( V_x > 0 \implies b_1 = 0 \)

- \( V_x = -0.984V + \frac{8}{82+6} \cdot 0.5V \)
  \[ V_x = -0.984V + 1V = 0.016V \]
  When \( b_2 = 1 \), \( V_x > 0 \) so \( b_2 = 0 \) and \( V_x \) is set back to \(-0.984V\) by switching \( b_2 \) back to ground.

- \( b_3 \) is switched:
  \[ V_x = -0.984V + \frac{1}{40} \cdot 0.5V = -0.484V \]
  \( V_x \) is now \( < 0 \) so \( b_3 = 1 \) and \( b_3 \) left connected to \( V_{\text{ref}} \).
by is switched:

\[ V_k = -0.98V + \frac{6.5V}{40} - 0.98V + 0.75V = -0.234V \]

\[ V_{x4} < 0 \Rightarrow b_4 = 1 \]

bs is switched:

\[ V_{x5} = -0.234V + \frac{1.5V}{40} = -0.107V \]

\[ V_{x5} < 0 \Rightarrow b_5 = 1 \]

May also be expressed from the drawing and the ois.

\[ \text{Sampled volt.}: \]

\[ \frac{32}{32+8} (-V_{in}) + \frac{7}{32+8} \cdot 5V = -0.984V + 0.75V = -0.109V \]

DAC: \( V_{out} = V_{ref} (b_1 \cdot b_2 \cdot b_3 \cdot b_4 \cdot b_5) = 0 \cdot 0 \cdot 1 \cdot 1 \cdot 1 \)

\[ V_{ref} = 5V \]

\[ \frac{SV}{2^5} = \frac{5V}{32} = 0.15625V \]

\[ V_{in} \]

\[ \rightarrow A/0 \]

\[ \rightarrow V_{io} \]

\[ \rightarrow V_x \]

\[ V_{out} = V_{ref} (b_1 \cdot b_2 \cdot b_3 \cdot b_4 \cdot b_5) = 0.125V + 0.0625V + 0.03125V = 0.21875V \]

\[ SV(0.21875) = 1.09375V \]

\[ V_a = \frac{1.09375V}{1.23V} \]

\[ = -0.13625 \]
Succ. Approx. Approach flow graph

Start

Signed input

Sample $V_n, V_{\text{DA}} = 0, i = 1$

$V_{in} > V_{\text{DA}}$

No

Yes

$b_i = 1$

$b_i = 0$

$V_{\text{DA}} \rightarrow V_{\text{DA}} + V_{\text{ref}}/2^{i+1}$

$V_{\text{DA}} \rightarrow V_{\text{DA}} - (V_{\text{ref}}/2^{i+1})$

$i \rightarrow i + 1$

No $i \geq N$

Yes

Stop

EX. 13.3 VIEWED IN ANOTHER WAY, AND WITHOUT PARASITICS.

10. mars 2010
Signed Charge redistribution A/D
(Fig. 13.8)

- Resembling the unipolar version (Fig. 13.7)
- Assuming $V_{\text{in}}$ is between $\pm V_{\text{ref}}/2$
- Disadvantage: $V_{\text{in}}$ attenuated by a factor 2, making noise more of a problem for high resolution ADCs
- Any error in the MSB capacitor causes both offset and a sign-dependent gain error, leading to INL errors
Resistor-Capacitor Hybrid (figure 13.9 in ”J & M”)

- First all capacitors are charged to $V_{\text{in}}$ before the comparator is being reset.
- Next a succ. approx. conversion is performed to find the two adjacent resistor nodes having voltages larger and smaller than $V_{\text{in}}$.
- One bus will be connected to one node while the other is connected to the other node. All of the capacitors are connected to the bus having the lower voltage.
- Then a successive approximation using the capacitor-array network is done, starting with the largest capacitor…
Speed estimate for charge-redistribution converters

- RC time constants often limit speed
- Individual time constant due to the 2C cap.: \((R_{s1}+R+R_{s2})2C\)
- \((R\ ; \ \text{bit line})\)
- \(\tau_{eq}=(R_{s1}+R+R_{s2})2^N C\), for the circuit in fig. 13.12
- For better than 0.5 LSB accuracy: \(e^{-T/\tau_{eq}} < 1/(2^N+1)\), \(T\) = charging time
  - \(T > \tau_{eq} (N+1) \ln 2\)
    - \(= 0.69(N+1)\tau_{eq}\)
- 30 % higher than from Spice simulations (”J & M”)
Algorithmic (or Cyclic) A/D Converter  (13.3)

- Similar to the Successive approximation converter
- Constant $V_{\text{ref}}$
- Doubles the error each cycle, instead of halving the reference voltage in each cycle, like succ. approx. conv.
- Requires an accurate multiply-by-2 amplifier
- Accuracy can be improved by operating in four cycles (instead of two)
- compact

\[
\begin{align*}
\text{Start} & \\
\text{Signed input} & \\
\text{Sample } V = V_{\text{in}}, i = 1 & \\
\text{No} & \\
V > 0 & \\
\text{Yes} & \\
b_i = 1 & \\
V \rightarrow 2(V - V_{\text{ref}}/4) & \\
\text{No} & \\
i \rightarrow i + 1 & \\
\text{Yes} & \\
\text{i > N} & \\
\text{Stop} & \\
\end{align*}
\]
Ratio-Independent Algorithmic Converter

- Simple circuitry
- Due to the cyclic operation the circuitry are reused in time
- Fully differential circuits normally used
Ratio-Independent Algorithmic Converter

1. Sample remainder and cancel input-offset voltage.
2. Transfer charge $Q_1$ from $C_1$ to $C_2$.
3. Sample input signal with $C_1$ again after storing charge $Q_1$ on $C_2$.
4. Combine $Q_1$ and $Q_2$ on $C_1$, and connect $C_1$ to output.

- The basic idea is to sample the input signal twice using the same capacitor. During the 2nd sampling the charge from the 1st capacitor is stored on a 2nd capacitor whose size is unimportant. After the 2nd sampling both charges are recombined into the 1st capacitor which is then connected between the opamp input and output.
- Does not rely on capacitor matching, is insensitive to amplifier offset.
Flash (Parallel) Converters (13.4)

- High speed – among the fastest
- $2^N$ comparators in parallel, each connected to different nodes – area consuming
- High power consumption
- Thermometer-code output fed into decoder
- Nands used for simpler decoding and error detection (bubble error)
- Differential comparator required to ensure sufficient PSSR
- Top and bottom resistors chosen to create the 0.5 LSB offset in an A/D converter
Flash converter

Any comparator connected to a resistor string node where $V_{ri}$ is larger than $V_{in}$ will have a 1 output.

One nano-gate will have a 0 output.

All other nano-gate outputs will be 1.

This also allows for error checking by checking for more than one 0 output.

(See fig. 18.1b, page 508)
Clocked CMOS comparator

- When the clock ("phi") is high, the inverter is set to its bistable point, $V_{in} = V_{out} (= V_{dd}/2)$. The other (left) side of $C$ is charged to $V_{ri}$.
- When the clock ("phi") goes low, the inverter switches, depending on the voltage difference between $V_{ri}$ and $V_{in}$. ($V_{ri} > V_{in}$: 1 output, $V_{ri} < V_{in}$: 0 output from inv.)
- Differential inverters helps poor PSRR with this simple comparator solution.

**Fig. 13.17** A clocked CMOS comparator.
Issues in Designing Flash A/D Converters

- **Input Capacitive Loading:** The large number of comparators connected to $V_{in}$ results in a large capacitive load on the input node which increases power and reduces speed.

- **Comparator Latch-to-Track Delay:** The internal delay in the comparator when going from latch to track mode.

- **Signal and/or Clock Delay:** Differences in signal/clock delay between the comparators may cause errors. Example: A250-MHz, 1-V peak input-sinusoid converted with 8-bit resolution requires a precision of 5ps. Can be reduced by matching the delays and capacitive loads on the signal/clock.

- **Substrate and Power-Supply Noise:** For an 8-bit converter with $V_{ref}=2V$ only 7.8mV of noise injection is required to introduce an error of 1LSB. The problem can be reduced by proper layout (Shielding, Differential clocks, Separate power supplies, and symmetrical layout).

- **Bubble Error Removal:** Comparator metastability may introduce wrong thermometer code (a single 1 or 0 in between opposite values).

- **Flashback:** Caused by latched comparators. When the comparator is switched from track to latch mode a charge glitch is introduced at the input. The problem is reduced by using a preamplifier and input impedance matching.
Two-Step (Subranging) A/D Converters (13.5)

- Popular choice for high-speed medium accuracy converters (8-10 b)
- Less area and power consumption than a Flash ADC
- The MSB’s are converted during the first step. In the next step the remaining error is converted into the LSB’s
- Speed is limited by the Gain Amplifier
- Requires N-bit accuracy for all components (May be relaxed by using Digital Error Correction)
Digital Error Correction for two-step A/D

- The accuracy requirements on the input ADC is relaxed due to the error corr.. 4-bit for MSb converter
Pipelined ADCs (13.5) Once the first stage has completed its work it immediately starts working on the next sample

• Small area

The pipelined ADC has its origins in the subranging architecture, first used in the 1950s. A block diagram of a simple 6-bit, two-stage subranging ADC is shown in Figure 11.

Figure 11. 6-bit, two-stage subranging ADC.

The output of the SHA is digitized by the first-stage 3-bit sub-ADC (SADC)—usually a flash converter. The coarse 3-bit MSB conversion is converted back to an analog signal using a 3-bit sub-DAC (SDAC). Then the SDAC output is subtracted from the SHA output, the difference is amplified, and this “residue signal” is digitized by a second-stage 3-bit SADC to generate the three LSBs of the total 6-bit output word.
Pipelined ADC - example

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Torge Normann Andersen, Bjørnar Hansen, Member, IEEE, Arild Rekormyr, Freda Telha, Johnny Bjersen, Member, IEEE, Thomas E. Bonnerud, and Øystein Moldover

Nominal sampling rate: 110MS/s
Technology: 0.18μm digital CMOS
Nominal supply voltage: 1.8V
Resolution: 12bit
Full scale analog input: 2Vpp
Area: 0.86mm²
Power consumption: 97mW
DNL: ±1.2 LSB
INL: -1.5+/±1.6 LSB
SNR (fC=10MHz): 67.1 dB
SNDR (fC=10MHz): 64.2 dB
SFDR (fC=10MHz): 69.4 dB
ENOB (fC=10MHz): 10.4 bit

Fig. 7. Power dissipation versus conversion rate. The input frequency and signal swing are 10 MHz and 2Vpp, respectively.

Fig. 9. SFDR, SNR, and SNDR versus input frequency. The conversion rate and signal swing are 110 MHz and 2Vpp, respectively.

Fig. 12. Figure of Merit (FM) versus 1/A for 12-bit ADCs. fC is given in MHz, A is given in mm² and P is given in mW

Digital circuitry: Delay elements and error correction

Switched-Capacitor Bias Generator
Reference Voltage Generator
Common Mode Voltage Generator

S/H and 1st stage
V_IN
C_H = 1.5pF
Scale: 1

2nd stage
C_H = 1pF
Scale: 2/3

3rd stage
C_H = 0.5pF
Scale: 1/3

10th stage

2 bit flash

2 12

IN

D_OUT

Power Dissipation (mW)

Conversion Rate (MS/s)

2 1 2 2

V1

R_C

V2

V1

V2

10000

100

10

0.1

0.01

1/A (mm²/μW)

0.001

Input Frequency (MHz)
• Very high speed (figure to the right from “Allen & Holberg”)
• $f_0$ is four timer higher than $f_1 - f_4$, which in addition is slightly delayed
• Only the S/H and the MUX must run on the highest frequency
• Tones are introduced at multiples of $f_0/N$
Time-Interleaved – best compromise between complexity and sampling rate – may be used for different architectures [Elbjornsson ’05]

Figure 7 Comparison between ADC architectures. The time-interleaved successive approximation ADC gives the best compromise between complexity and sampling rate.
Dynamic range

• Dynamic range is defined as the power of the maximum input signal range divided by the total power of the quantization noise and distortion
• Often referred to as **Signal-to-Noise-and-Distortion** range
• $S/(N+D)$
• **SINAD**
Analog and digital supply voltages are reduced as technology scales

Some ADC trends:

- Limited dynamic range at low supply voltages remains the utmost challenge for high-resolution Nyquist converters.
- Oversampling converters will dominate this arena in the future.
- Linearity correction with digital correction is becoming prevalent.

Fig. 1. Scaling of supply and threshold voltages.

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submieron CMOS

Y. Chiu 1, B. Nikolić 2, and P. R. Gray 2
1 Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
2 Electrical Engineering and Computer Sciences, University of California at Berkeley
Nyquist ADCs at ISSCC; FOM, Effective Number of Bits

\[ \text{FOM} = \frac{p}{2^{\text{ENOB}} f_s} \]

- **FOM**: Figure of Merit
- High-resolution conv.: FOM minimum at about $10^{-17}$ J/step
- 6-bit ADCs: FOM about 4 orders of magnitude worse than 14 bit converters, suggesting that there is much to be gained by designing more efficient 6-bit ADCs
- Better ENOB reported for 350 nm than 250 nm, 180 nm and 130 nm
- Data from ISSCC up to 2005.

**Fig. 22.** FOM as a function of effective number of bits and technology.

**Analog Circuit Design in Nanoscale CMOS Technologies**

Classic analog designs are being replaced by digital methods, using nanoscale digital devices, for calibrating circuits, overcoming device mismatches, and reducing bias and temperature dependence.

By Larry L. Leshy, Life Senior Member IEEE, Trond Vigestad, Senior Member IEEE, Carsten Wulff, Member IEEE, and Kenneth Martin, Fellow IEEE

10. mars 2010
Nyquist ADCs at ISSCC; FOM, Sampling rate

FOM = \frac{P}{2^{2\text{ENOB}} f_s}.

- Maximum Sampling frequency (Usually faster is better) and FOM.
- ISSCC 2000-2007 (90 nm, 130 nm, 180 nm technologies)
- Small improvement in sampling frequency in going to finer technologies, mainly due to reduced capacitance.
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<th>Publication year</th>
<th>SFDR @ Nyquist [dB]</th>
<th>ENOB @ Nyquist</th>
<th>Nyquist update rate, [Ms/s]</th>
<th>Power consumpt. [mW]</th>
<th>Area [mm²]</th>
<th>Supply voltage [V]</th>
<th>Technology [nm]</th>
<th>other</th>
<th>Reference</th>
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<td>130</td>
<td>Time interleaved</td>
<td>Gupta et al, IEEE JSSC ’06</td>
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<td>Time interleaved succ. approx</td>
<td>Ginsburg et al, IEEE JSSC ’07</td>
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<td>2007</td>
<td>8</td>
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<td>180</td>
<td>Switched opamp pipelined</td>
<td>Wu et al, IEEE JSSC ’07</td>
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<td>2008</td>
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<td>Li et al, IEEE JSSC ’08</td>
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<td>2009</td>
<td>81</td>
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<td>0.073</td>
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<td>180</td>
<td>Delta-sigma</td>
<td>Chae, JSSCC Feb.09</td>
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<td>&quot;folding flash&quot;</td>
<td>Verbruggen, JSSCC, Mar. ’09</td>
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<td>350</td>
<td>Continuous time sigma delta</td>
<td>TCAS-II, Jan. ’09</td>
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10. mars 2010
Sampling-time uncertainty

• Variation in output voltage caused by variations in the time of sampling

Consider the following input signal:

\[ V_{in} = \frac{V_{ref}}{2} \sin(2\pi f_{in} t) \]

If the variation in sampling time is \( \Delta t \), following equation must be satisfied to keep \( \Delta V \) less than 1LSB

\[ \Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \]
Additional literature

- D. M. Gingrich: Lecture Notes, University of Alberta, Canada
- Walt Kester: Which ADC is right for your application?
- Lecture Notes, University of California, Berkeley,
  EE247 Analog Digital Interface Integrated Circuits, Fall 07; http://inst.eecs.berkeley.edu/~ee247/fa07/

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A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Norveide Andersen, Bjornar Hemes, Member, IEEE, Atle Briskemyr, Frode Tesnæs, Johnny Bjoerensen, Member, IEEE, Thomas E. Bonnerud, and Øystein Molbøvør
Next Tuesday (10/3-08):
Rest of chapter 13.
• Chapter 14 Oversampling Converters

Figure 1. ADC architectures, applications, resolution, and sampling rates.

Figure 6. Noise-spectrum effects of the fundamental concepts used in Σ-Δ: oversampling, digital filtering, noise shaping, and decimation.
“…The ratio between two similar components on the same integrated circuit can be controlled to better than +/- 1 %, and in many cases, to better than +/- 0.1 %. Devices specifically constructed to obtain a known, constant ratio are called matched devices.”

“Matching – the Achilles Heel of Analog” (Chris Diorio)
Some companies located in Norway, doing (or that have done) full custom data converter designs:

- Analog Concepts (Trondheim)
- Arctic Silicon Devices (Trondheim)
- Atmel Norway (Trondheim)
- Energy Micro (Oslo)
- GE Vingmed Ultrasound (Horten)
- Nordic Semiconductors (Trondheim, Oslo)
- Novelda (Oslo)
- Micrel (Oslo)
- Sintef (Trondheim, Oslo)
- Texas Instruments (Oslo)
Metastability in FFs (http://www.asic-world.com/tidbits/metastability.html) To avoid M. in comparators: Make gain high, increase current levels.

What is metastability?
Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable; this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either ‘1’ or ‘0’. This whole process is known as metastability. In the figure below Tsu is the setup time and Th is the hold time. Whenever the input signal D does not meet the Tsu and Th of the given D flip-flop, metastability occurs.

The approximate equation which describes the output voltage, $V_O(t)$ is given by:

$$V_O(t) = \Delta V_{IN}/Ae^{t^1/\tau},$$

Eq 1

where $\Delta V_{IN}$ – the differential input voltage at the time of latching, $A$ – the gain of the preamp at the time of latching, $\tau$ = regeneration time constant of the latch, and $t$ = the time that has elapsed after the comparator output is latched (see References 2 and 3).

For small differential input voltages, the output takes longer to reach a valid logic level. If the output data is read when it lies between the “valid logic 1” and the “valid logic 0” region, the data can be in error. If the differential input voltage is exactly zero, and the comparator is perfectly balanced at the time of latching, the time required to reach a valid logic level can be quite long (theoretically infinite). However, comparator hysteresis and input noise makes this condition highly unlikely. The effects of invalid logic levels out of the comparator are different depending upon how the comparator is used in the actual ADC.

From a design standpoint, comparator metastability can be minimized by making the gain (A) high, minimizing the regeneration time constant ($\tau$) by increasing the gain-bandwidth of the latch, and allowing sufficient time ($t$), for the output of the comparator to settle to a valid logic level. It is not the purpose of this discussion to analyze the complex tradeoffs between speed,

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