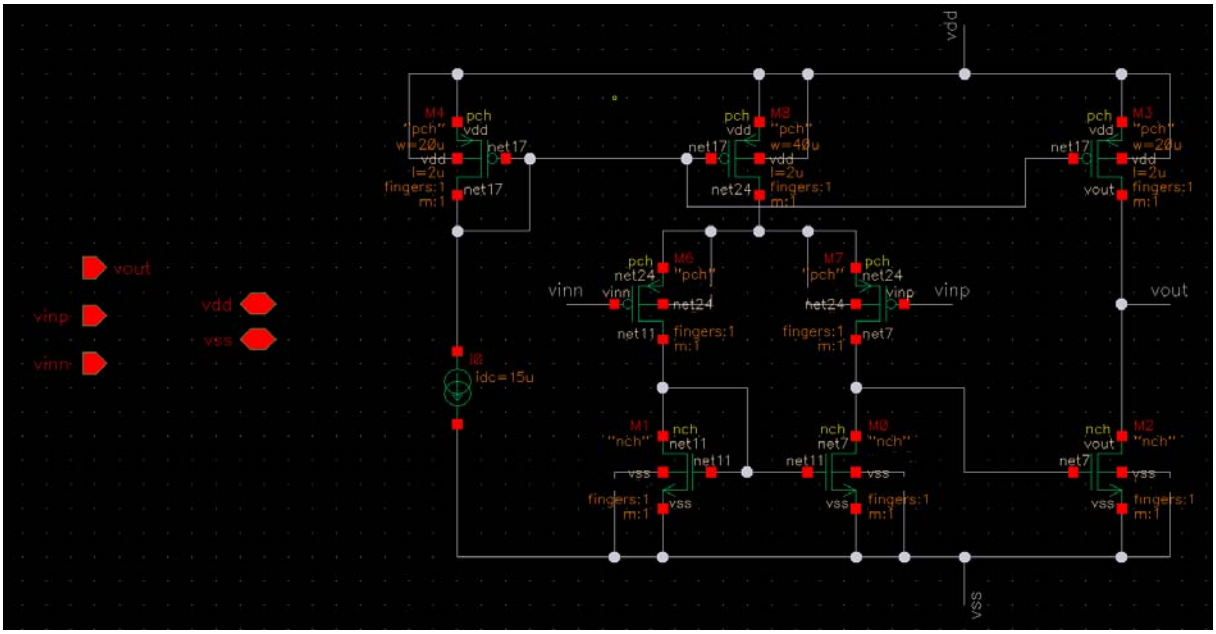
Comparators Simulating (not applied to the latched comparator)

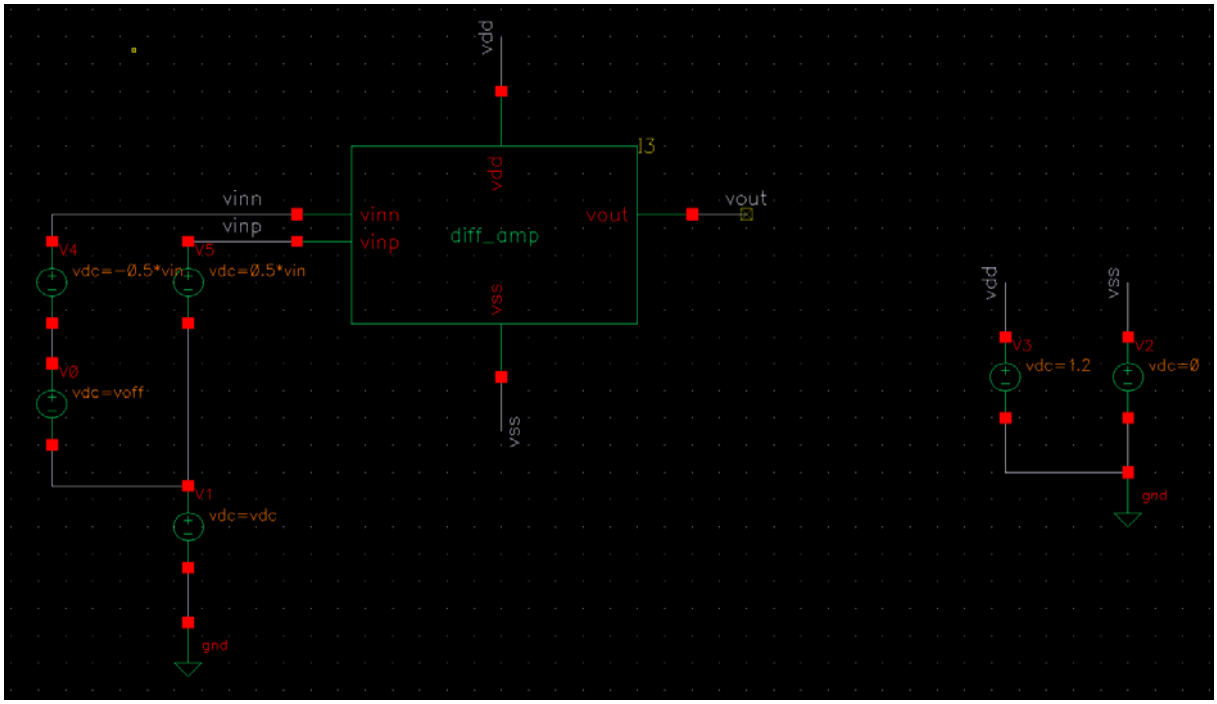
Schematic of Comparator (without any optimization, not recommended to use for your project):



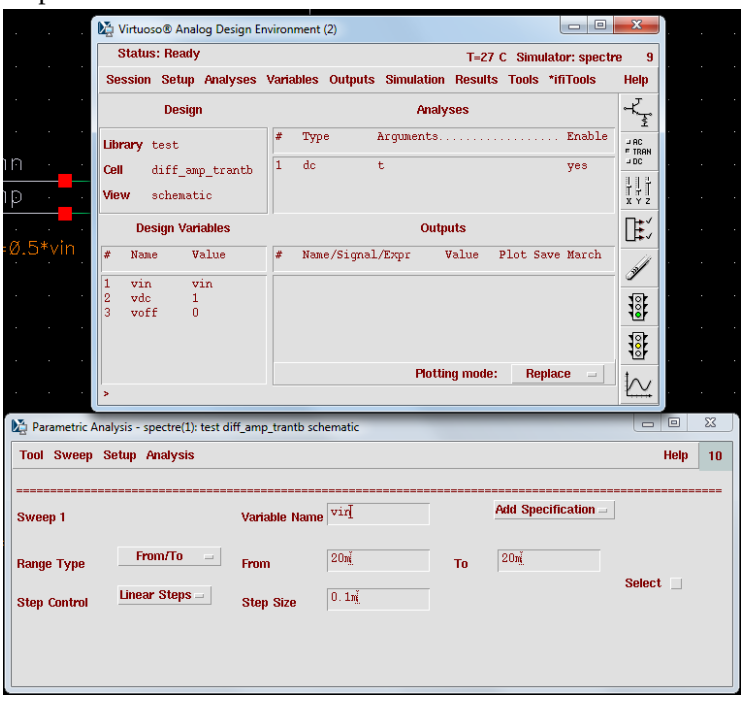
1) DC gain and DC Offset

You can find the testbenches in project library (INF4420Project)

Testbench (diff_amp_dctb):

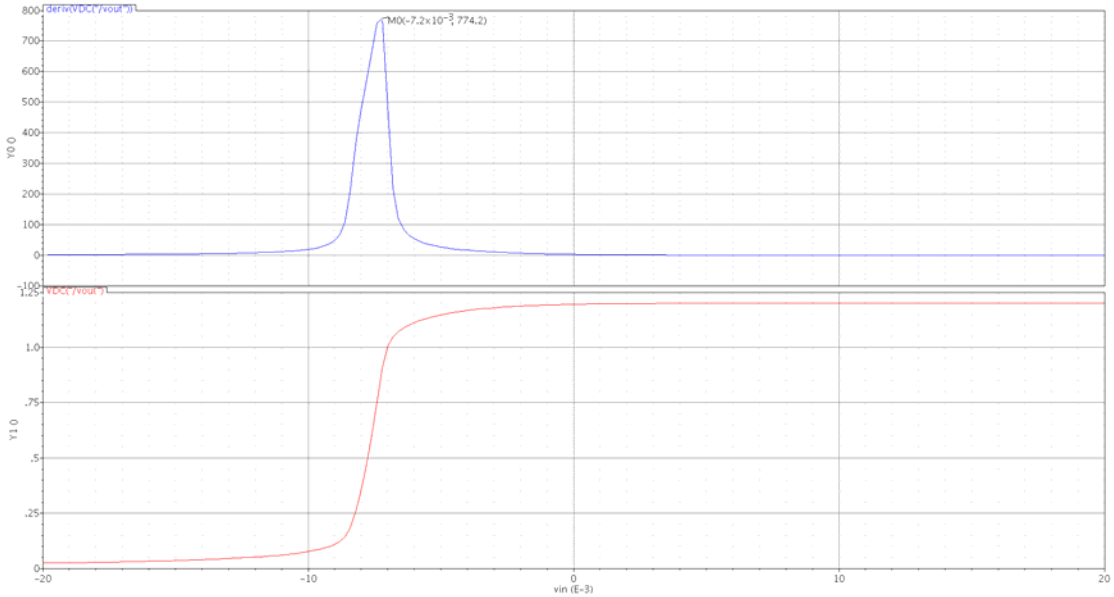


Set “voff” to 0V. Sweep the “vin” at different “vdc”.



In this tutorials, we assume the input range is from 0.2V to 1V.

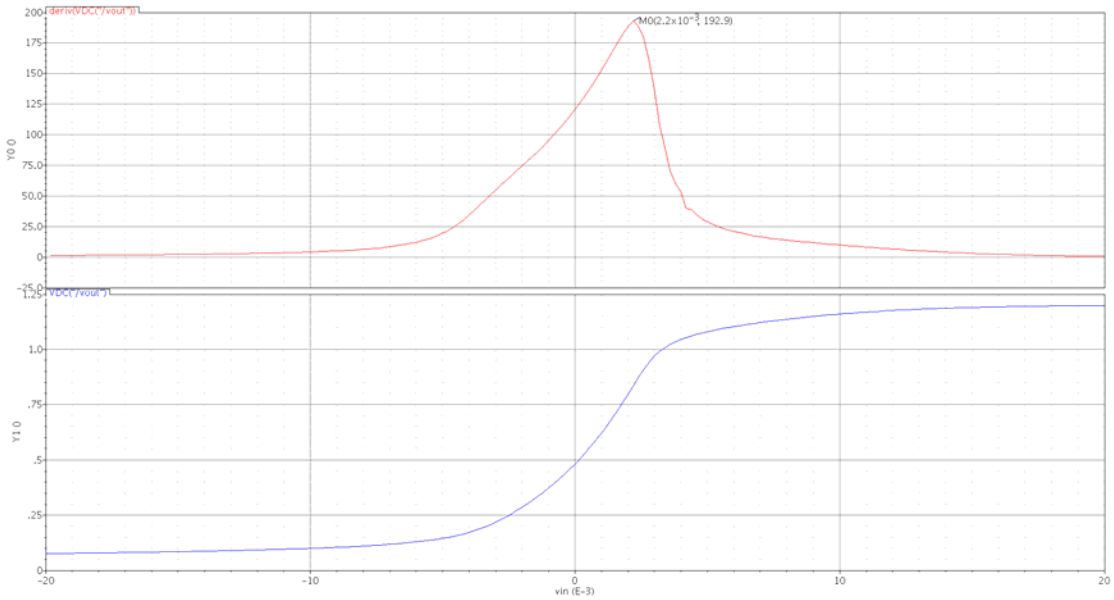
When vdc = 1V (make sure the step size is small enough to see smooth curves),



DC gain = 774.2
Offset = -7.2mV

Since we are using PMOS input pair, when the input voltage is too high, the input pair (M6-M7) will enter go to weak-inversion region and the current mirror transistor M8 will enter triode region, this increases the offset.

When vdc = 0.2V,



DC gain = 192.9
Offset = 2.2mV

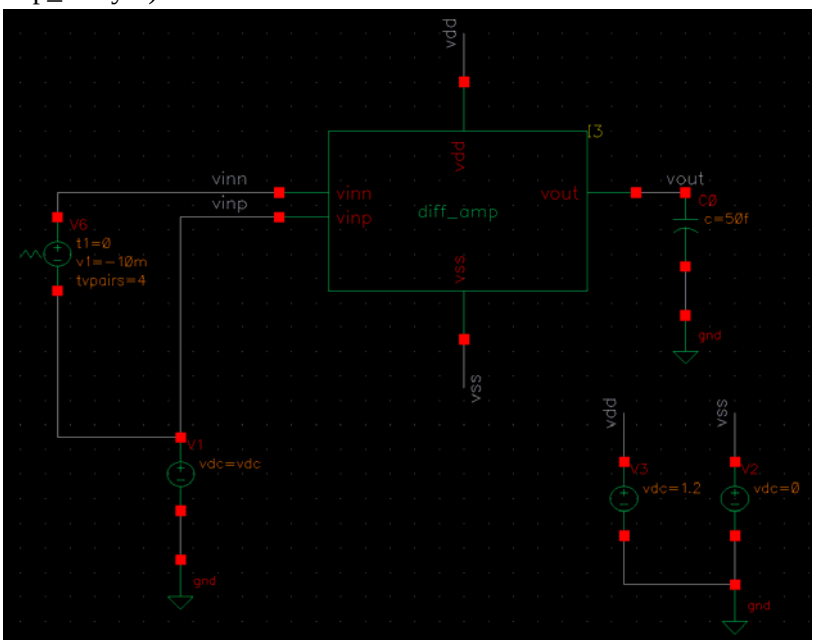
Notice that V_{DS} of M0 and M1 is one V_{GS} (since M1 is diode-connected). When vin is too small, the V_{DS} of M6 and M7 is too small to make them operating in saturation region. g_m and the gain are hence

reduced. To solve this, you can add more stages to increase the gain. Or change your topology to folded cascode.

You can see that the DC biasing conditions, hence, the DC gain and the offset are changed with the input common mode voltage. Make sure your comparator can meet the spec for the entired input range. (at least show us it does for the minimum and maximum input voltage, i.e. 200mV and 1V in this example)

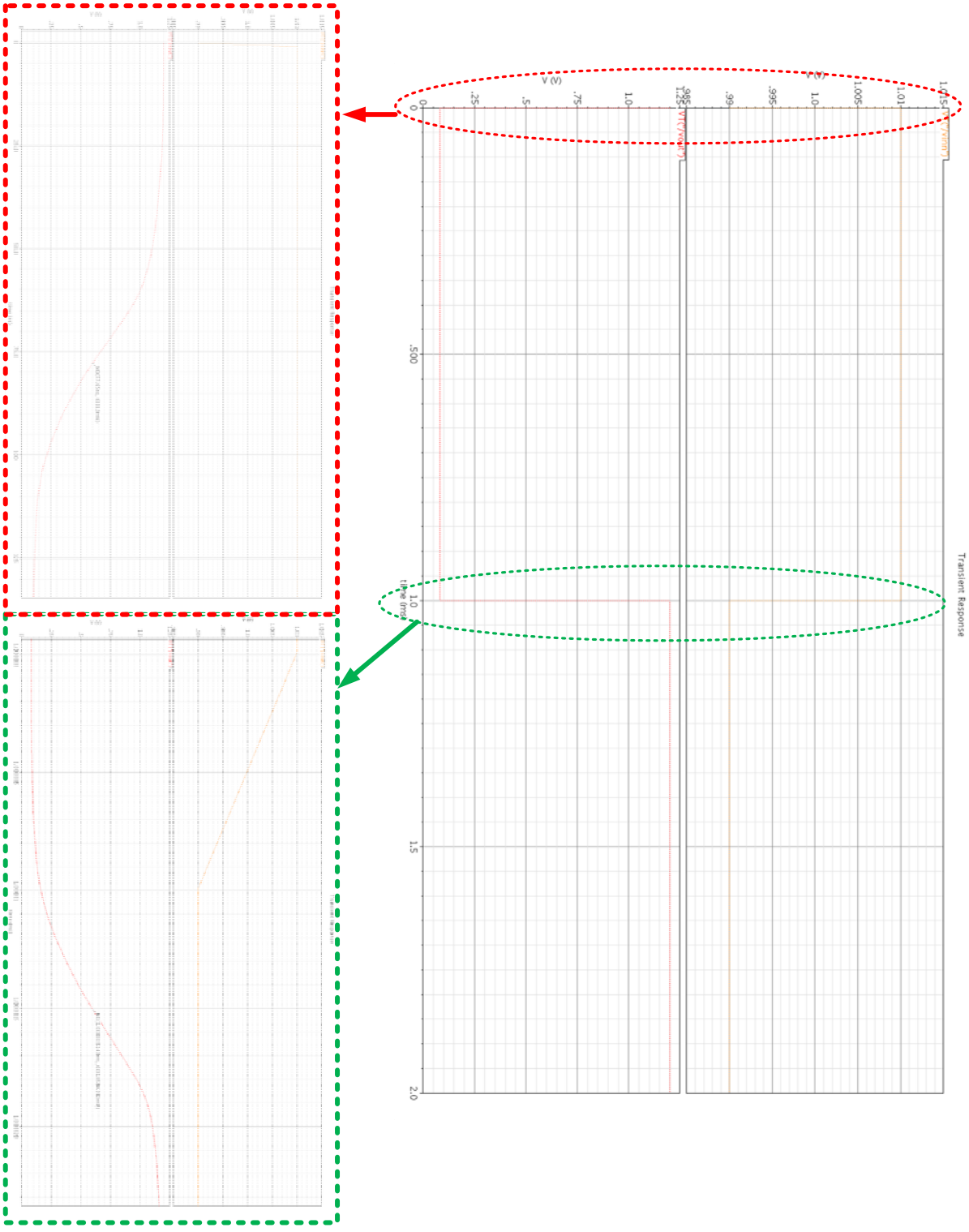
2) Delay Simulation

Testbench (diff_amp_delaytb):



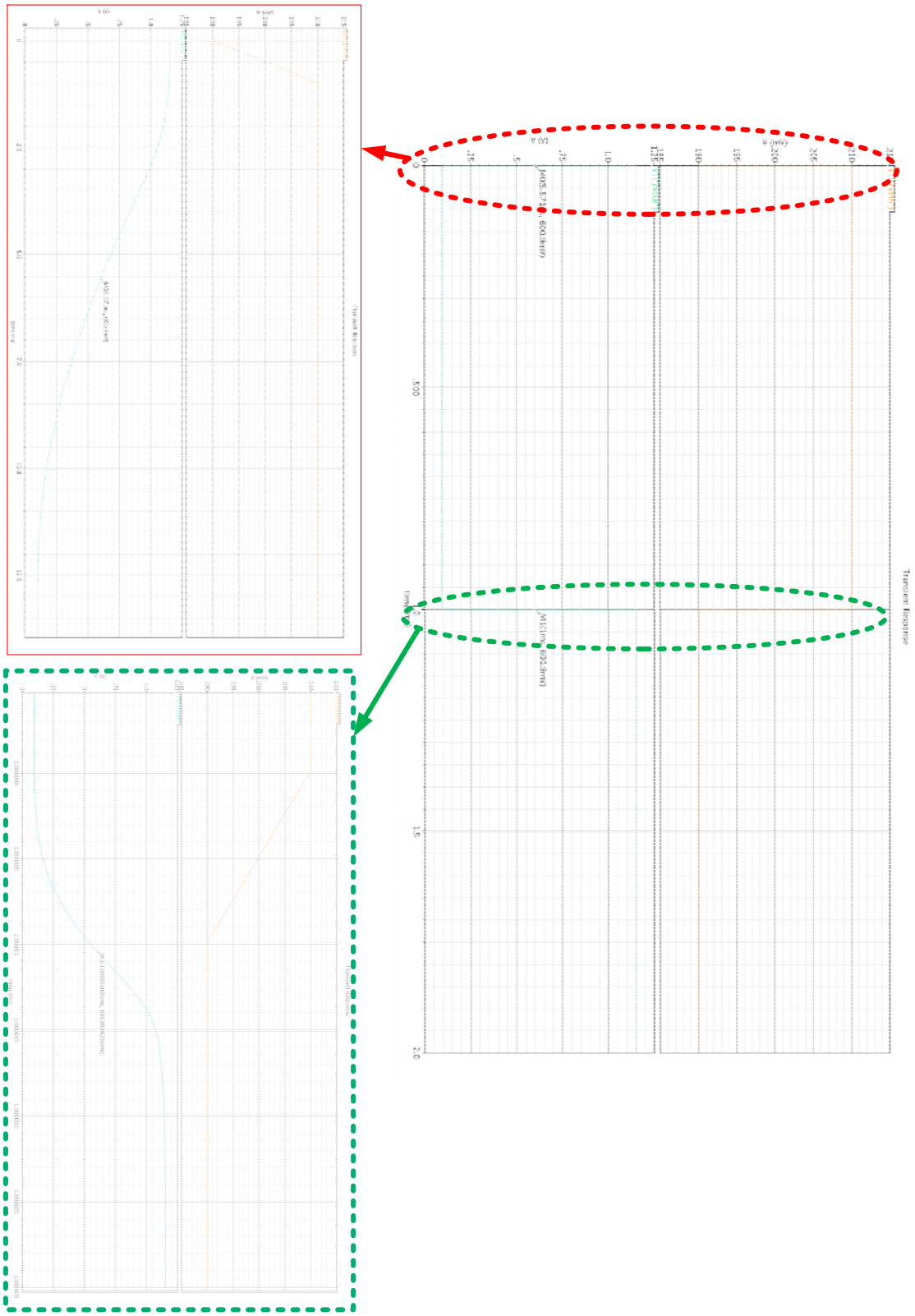
Set the “vdc” and input a small-amplitude square wave to the “vinn” (20mV in this example)

When vdc = 1V,



The delay is 77 ns

When vdc = 0.2V,



The delay is 10.49 ns.

Again, delay is changed with the input common mode voltage. Make sure your comparator can meet the spec for the entired input range.