INF4420 Project Spring 2011

Successive Approximation Register (SAR)
Analog-to-Digital Converter (ADC)

1. Introduction

Data converters are one of the fundamental building blocks in integrated circuit design. Their purpose is to interface the analog and digital domains. Data converters can be realized in many different ways and SAR ADC is one common topology for low-frequency applications. A block diagram of a SAR ADC is shown in Fig. 1, which consists a DAC, sample and hold, comparator and digital circuitries.

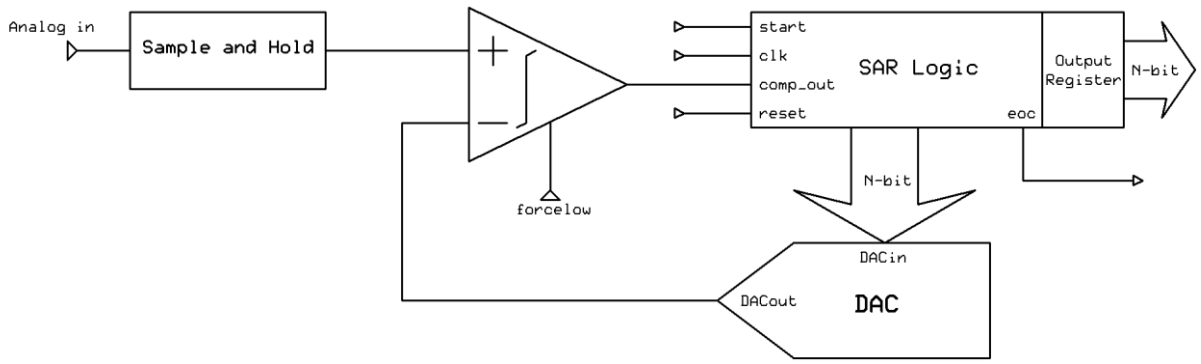

Fig. 1 Block diagram of a SAR DAC.

Your company is starting a project to design a SAR ADC using a TSMC 90 nm process with the following spec:

1) Sampling rate: 500 kHz
2) Resolution ≥ 6 bits
3) V_{DD} = 1.2 V
4) No missing codes
5) Monotonic

Your work colleague K has finished the system level simulation and modeling using verilog-A and your boss S is asking you to design the DAC and the comparator. Based on the K's simulations results, the DAC and the comparator have to achieve the following spec:

DAC Spec:

1) Topology: R-string
2) Sampling rate: 7 MHz
3) Resolution $\geq$ 6 bits
4) V_{DD} = 1.2 V
5) DNL < ±0.5 LSB
6) INL < ±0.5 LSB
7) $V_{out,p\text{-}p} \geq$ 600 mV
8) C_{LOAD} = 50 fF

Comparator Spec:

1) Delay $\leq$ 0.5 clock cycle
2) V_{DD} = 1.2 V
3) Offset < 0.5 LSB
4) Input range: Work properly with the whole swing of your DAC. Pay attention to choose your input transistor type.
5) Gain > $V_{DD}/(V_{ref}/2^n)$ for all input common-mode voltage (remember your input common-mode voltage, hence your biasing condition, is changing with the DAC output).
6) C_{LOAD} = 50 fF

K put the ideal components on: /projects/nano/kurs/INF4420/INF4420Project, you can use them for verifying your circuits. Notice that K is also a newbie, you may find some errors on the spec. Feel free to tell K if you find any mistake.

2. Assignments

**** Notice that the workload in this project is intended for groups consisting of two students!!! ****

Assignment 1: Design a testbench for the DAC and SAR ADC introduction

1) Make a suitable testbench for the DAC. This can be done by either digital logic or verilog-A (Verilog-A is recommended but not compulsory).

2) Write a small report (2 pages maximum) regarding the SAR ADC architecture and include the following in your report:
   - Describe the functionality of a typical SAR ADC architecture.
   - Pros and cons of the SAR ADC architecture.
   - Other aspects that may be relevant.

   (This part may be included in your final report as parts of the introduction or similar)

3) Get yourself familiar with the supplied SAR ADC components.

4) K is on leave now and the building block model of the *output register* is lost. Try to implement the *output register* using the supplied (ideal) building blocks.

Assignment 2: DAC and comparator design

Design the DAC and comparator based on the spec mentioned above. You may assume you have ONE 1 μA current source available for biasing.

Some hints to improve score.

1) Record all the reasons and statements to support your decisions. Trial and error approach will not make S happy.
2) Show your design can meet the spec with PVT (Process, Voltage and Temperature) variation. Although it is not required in this project, but it will give higher yield in the real life and S can earn more money.

Assignment 3: Implementation of DAC into SAR ADC

Implement your DAC design into the SAR ADC topology. Make necessary modifications to the ideal components if your implementation has higher specifications then the minimum (for example resolution).

Assign a ramp up signal to the ADC input and verify that you get corresponding digital values on the ADC output.

3. Project requirements

Group members must jointly go through the project description and assign work assignments. It must be made visible in the report how the distribution of work has been assigned throughout the project. The following (*but not limited to*) tasks must be addressed before the project can be regarded as complete:

1) It is expected that all circuits/sub-circuits have a schematic and appropriate symbol. The final DAC should be made up of a single symbol.

2) After the DAC schematic is complete and all simulation results (including Monte Carlo simulations) are satisfactory, a layout of the complete system must be made. There are certain issues that are often encountered when doing analog/mixed-signal layout. Find out what they could be and describe them in your final report. Make an effort to implement countermeasures.

3) When you have completed the layout, run Design Rule Check (DRC) and Layout Versus Schematic (LVS). These checks have to be free of errors. The LVS output log must be included in the final report as an appendix.

4) The next step is to do back annotation of parasitic components (R and C) to the schematic view, or parasitic extraction as it is also called. This will result in a netlist with parasitic resistances and capacitances.

5) On the basis of the extracted netlist, you may now do post layout simulations (Monte Carlo simulations included). Her you must carry out the appropriate simulations and compare them with the previous simulation results that were solely based on the schematics.

4. Report requirements

The final report may be written it the text editor of your choice, but the report must be well organized and easy to read. All central aspects of the project must be supplied by relevant figures and plots. It is important to document/justify the choices you make regarding both the schematic and layout. (Important topics may be; matching, transistor dimensions, choice of components etc.) Plots of all the schematics and the layout, with clearly visible parameters such as dimensions must be included as an appendix for all circuits/sub circuits. References

that you may have used in the project must also be included. All schematics and layouts must be made available for inspection, with the exact directory path specified in your final report. Everything must be understandable just from reading the final report.

5. Submissions and approvals.

Assignment 1. Mandatory hand-in.

- Schematic (approved by lab advisor) Deadline February 18.

Assignment 2.

- Schematic (approval by lab advisor) Deadline March 18.
- Layout (approval by lab advisor) Deadline April 13.

Assignment 3. Deadline April 27.

Final Report. Deadline May 4.

Deadlines may be changed, pay attention to the course website.

6. Remarks

- Do some hand calculations, or at least predict the results before you do simulations. Simulations without any thinking will only give you doubts, not answers.
- Try to use top-down design approach.
- If you find problems on your layout, correct them as early as possible!
- Make sure you have think throughly and carefully before you come to ask us questions.

☺ Good luck and enjoy!!! ☺