Please read the figure below CAREFULLY!!! Before you start the whole system simulation, you need to modify the top schematic a bit, see the following figures.



Tips for Doing Large Simulations:

Simulation results should be saved in local computer

When you are doing a large simulation, you may want to store your simulation data in the local machine instead of your personal account which has very limited space. You can do this by:

Go to "Setup" then "Simulator/Directory/Host". Change the Project Directory to "/tmp"

🗖 Choosing Simulator/Directory/Host Virtuoso® Analog 🗕 🗆 🗙					
ок	Cancel	Defaults		Help	
Simulator		spect	re 🗆		
Project Directory		/tmp]			
Host Mode		🔶 local	\diamondsuit remote $\ \diamondsuit$ distributed		
Host					
Remote Directory					

Select the signals you want to save

Cadence will save all the node voltages by default, but you may not be interested at most of them. Instead you can select which nodes you want to monitor, it can be done by:

1) Go to "Output" in Analog Design Environment and click "save all".

2) Enable "Selected" for "Select signals to output (save)"

Then Cadence will save only the signals you have been selected in Analog Design Environment.

Alternatively, you can select saving the signals in a hierarchy ways.

1) Go to "Output" in Analog Design Environment and click "save all".

2) Enable "lvl" for "Select signals to output (save)"

3) Set "Set level of subcircuit to output" to "1". Now, you are saving all the node voltages from the top level to one level down from the top level. See the figure below. If you want to save the signals on the top level schematic, then "Set level of subcircuit to output" should be set to "0".

Nave Options	×
OK Cancel Defaults Apply	Help
Select signals to output (save)	_ none _ selected _ lvlpub 🔳 lvl _ allpub _ all
Select power signals to output (pwr)	🗌 none 🔄 total 🔄 devices 🔄 subckts 🔄 all
Set level of subcircuit to output (nestlvl)	1
Select device currents (currents)	selected nonlinear all
Set subcircuit probe level (subcktprobelvl	
Select AC terminal currents (useprobes)	yes no
Select AHDL variables (saveahdlvars)	🔄 selected 🛄 all
Save model parameters info	—
Save elements info	•
Save output parameters info	•
Save primitives parameters info	•
Save subckt parameters info	
Save asserts info	