Sampling switches, charge injection, Nyquist data converter fundamentals

Tuesday, February 8th, 9:15 – 11:35

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Last week – Tuesday, February 1st

11.1 General considerations
11.2 Supply-independent biasing
11.3 Temperature-independent References
- 11.3.1 Negative TC-voltage
- 11.3.2 Positive TC-voltage
- 11.3.3 Bandgap reference

11.4 PTAT Current generation
11.5 Constant-Gm Biasing

12.2 Sampling Switches
12.3 Switched Capacitor amplifiers

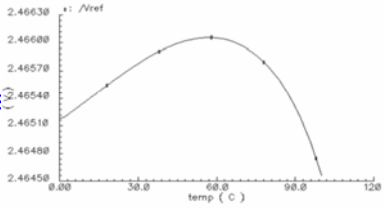

Figure 4 Output reference Verf vs. temperature.

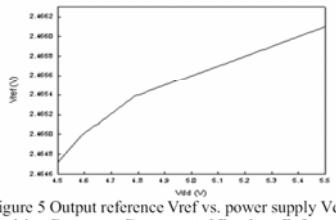

Figure 5 Output reference Vref vs. power supply Vdd.

A High Precision Curvature Compensated Bandgap Reference without Resistors

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Institute of Microelectronics, Peking University, Beijing 100871, P. R. China
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Today, February the 8th

- 12.2 Sampling switches
- 12.2.1 MOSFETS as Switches
- 12.2.2 Speed considerations
- 12.2.3 Precision considerations
- 12.2.4 Charge injection cancellation
- 12.3 Switched-Capacitor Amplifiers
- 12.3.1 Unity-Gain Sampler / buffer
- 12.3.2 Noninverting amplifier
- 12.3.3 Precision Multiply-by-Two Circuit
- 12.4 Switched-Capacitor Integrator
- 12.5 SC common-mode feedback
- Data converter fundamentals ("Maloberti"++)

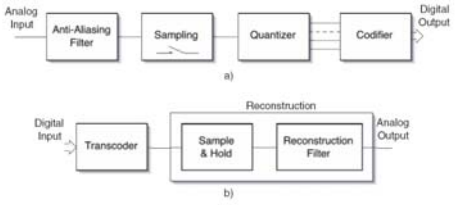
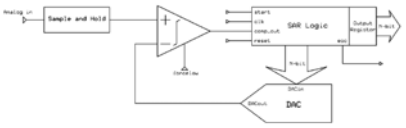


Figure 1.1. Block diagram of the basic functions of an A/D (a) and a D/A (b) converter.



Track (/sample-) and Hold capabilities of a sampling circuit

12.2 in "Razavi")

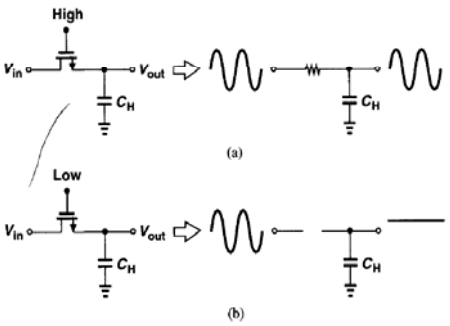


Figure 12.10 Track and hold capabilities of a sampling circuit.

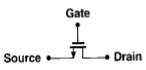
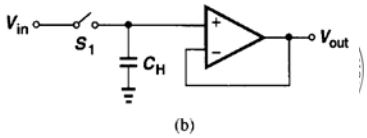


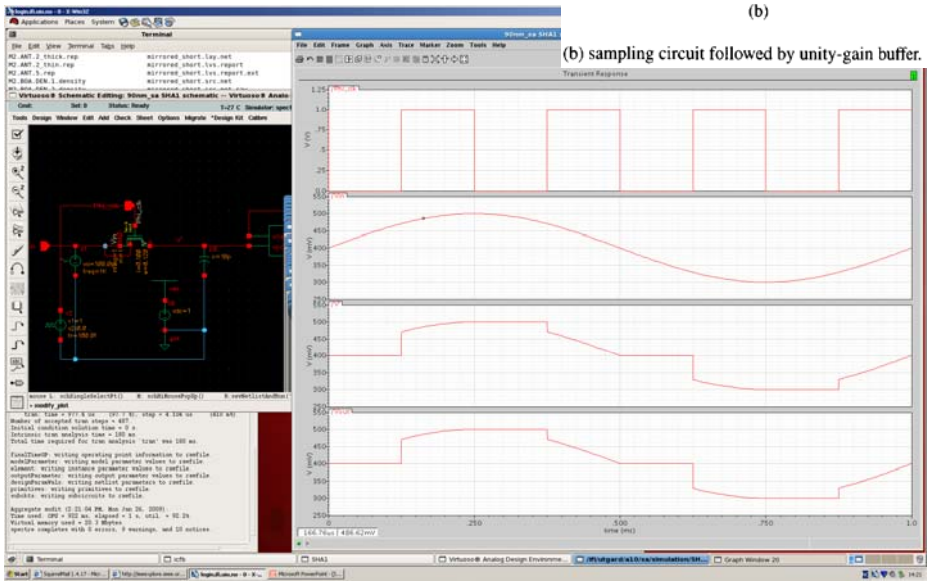
Figure 2.1 Simple view of a MOS device.

S/H signals (clk, V_{in}, $V_{CH,}$ V_{out})

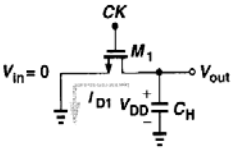


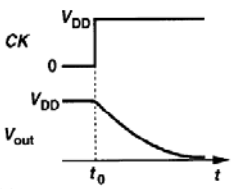
(b)

(b) sampling circuit followed by unity-gain buffer.



Track (/sample-) and Hold capabilities of a sampling circuit 1/2 (ch. 12.2 in "Razavi")





(a)

- CK goes high at t=t_0. $V_{in} = 0$ for t ≥ 0. C_H initially has a voltage equal to V_{dd}.
- At t=t_0 M_1 operates in saturation, but falls into the triode region after some time, when $V_{out} = V_{dd} - V_{TH}$. Discharging continues until V_{out} approaches zero.
- Current when in saturation:

$$I_{D1} = (\mu_n C_{ox}/2)(W/L)(V_{DD} - V_{TH})^2$$

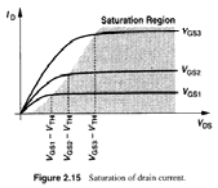
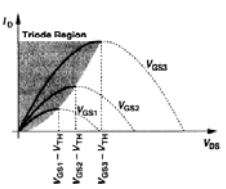


Figure 2.15 Saturation of drain current.



If $V_{DS} \leq V_{GS} - V_{TH}$, we say the device operates in the "triode region."[5]

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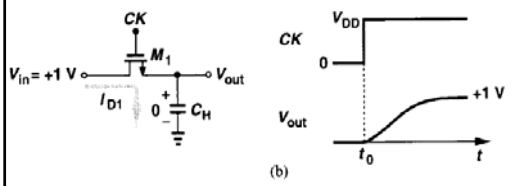
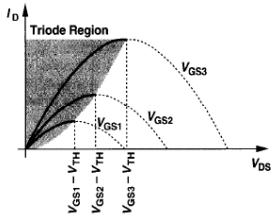
Track (/sample-) and Hold capabilities of a sampling circuit II/II (ch. 12.2 in "Razavi")





- CK goes high at t=t_0, when V_{out} = 0 V, and V_{dd} = 3 V.
- M_1's source is connected to C_H,and the transistor turns on with V_{GS} = 3 V, but V_{DS} = 1 V. Thus, M1 operates in the triode ("linear") region, charging C_H until V_{out} appoaches 1 V.

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A couple of observations regarding the MOS switch

(ch. 12.2 in "Razavi")

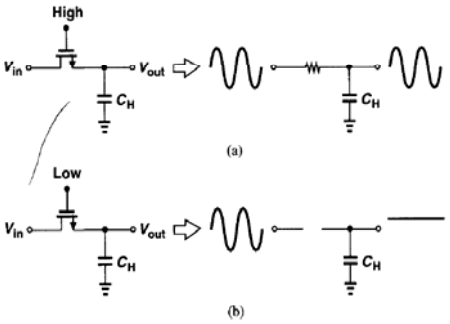
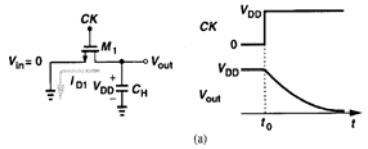


Figure 12.10 Track and hold capabilities of a sampling circuit.

- We have seen that a MOS switch can conduct current in either direction simply by exchanging the role of the source and drain terminals.
- When the switch is on, V_{out} follows V_{in}.
- When the switch is off, V_{out} remains constant (Fig 12.10 b)).

8

(Ex. 12.2 in "Razavi") Vout as as a function of time, for Fig. 12.9 a) (λ = 0)



Solution

Before V_{out} drops below $V_{DD} - V_{TH}$, M_1 is saturated and we have:

$$V_{out}(t) = V_{DD} - \frac{I_{D1}t}{C_H}$$
$$= V_{DD} - \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{TH})^2\frac{t}{C_H}.$$

After

$$t_1 = \frac{2V_{TH}C_H}{\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{TH})^2}, \quad (12.9)$$

M_1 enters the triode region, yielding a time-dependent current. We therefore write:

$$C_H\frac{dV_{out}}{dt} = -I_{D1} \quad (12.10)$$
$$= -\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{DD} - V_{TH})V_{out} - V_{out}^2, big\right] \quad t > t_1. \quad (12.11)$$

Rearranging (12.11), we have

$$\frac{dV_{out}}{[2(V_{DD} - V_{TH}) - V_{out}]V_{out}} = -\frac{1}{2}\mu_n\frac{C_{ox}}{C_H}\frac{W}{L}dt, \quad (12.12)$$

which, upon separation into partial fractions, is written as

$$\left[\frac{1}{V_{out}} + \frac{1}{2(V_{DD} - V_{TH}) - V_{out}}\right]\frac{dV_{out}}{V_{DD} - V_{TH}} = -\mu_n\frac{C_{ox}}{C_H}\frac{W}{L}dt. \quad (12.13)$$

Thus,

$$\ln V_{out} - \ln[2(V_{DD} - V_{TH}) - V_{out}] = -(V_{DD} - V_{TH})\mu_n\frac{C_{ox}}{C_H}\frac{W}{L}(t - t_1), \quad (12.14)$$

that is,

$$\ln\frac{V_{out}}{2(V_{DD} - V_{TH}) - V_{out}} = -(V_{DD} - V_{TH})\mu_n\frac{C_{ox}}{C_H}\frac{W}{L}(t - t_1). \quad (12.15)$$

Taking the exponential of both sides and solving for V_{out}, we obtain

$$V_{out} = \frac{2(V_{DD} - V_{TH})\exp\left[-(V_{DD} - V_{TH})\mu_n\frac{C_{ox}}{C_H}\cdot\frac{W}{L}(t - t_1)\right]}{1 + \exp\left[-(V_{DD} - V_{TH})\mu_n\frac{C_{ox}}{C_H}\cdot\frac{W}{L}(t - t_1)\right]}. \quad (12.16)$$

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Maximum output of NMOS S/H (ch. 12.2 in "Razavi", pp. 412)

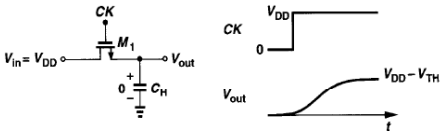
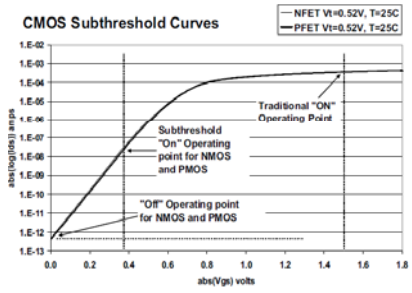


Figure 12.11 Maximum output level in an NMOS sampler.



- Assume $V_{in} = V_{dd}$ (for the circuit from Fig. 12.9 b))
- Vgs = Vdd, initially . $V_{DS} = V_{DD}$ → $V_{DS} \geq V_{GS} - V_{TH}$; saturation
- T goes, V_{out} → $V_{DD} - V_{TH.}$ (since the "overdrive" voltage vanishes and the current available for charging C_H go to negligible values)
- But: Given enough time, V_{out} will approach V_{DD}, due to subthreshold currents conducted by the transistor.
- Serious limitation: If the input signal is close to V_{DD}, the output provided by an NMOS switch cannot track the input (fast enough – remember subthreshold conduction).
- Similar problem with PMOS.

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Ex. 12.3 R_{on} variation in sampling switch (ch. 12.2 in "Razavi")

Example 12.3

In the circuit of Fig. 12.12, calculate the minimum and maximum on-resistance of M_1. Assume $\mu_n C_{ox} = 50\ \mu A/V^2$, $W/L = 10/1$, $V_{TH} = 0.7$ V, $V_{DD} = 3$ V, and $\gamma = 0$.

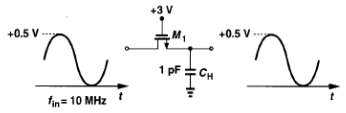


Figure 12.12

Solution

We note that in the steady state, M_1 remains in the triode region because the gate voltage is higher than both V_{in} and V_{out} by a value greater than V_{TH}. If $f_{in} = 10$ MHz, we predict that V_{out} tracks V_{in} with a negligible phase shift due to the on-resistance of M_1 and C_H. Assuming $V_{out} \approx V_{in}$, we need not distinguish between the source and drain terminals, obtaining

$$R_{on1} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{TH})}. \quad (12.22)$$

Thus, $R_{on1,max} \approx 1.11$ kΩ and $R_{on1,min} \approx 870\ \Omega$. By contrast, if the maximum input level is raised to 1.5 V, then $R_{on1,max} = 2.5$ kΩ.

- Time for the output to settle within a given accuracy (ex. 0.1 %) depends on the input voltage (T= R_{ON}C).
- MOS devices operating in deep triode region are sometimes called zero-offset switches to emphasize that they exhibit no dc shift between the input and output voltages.
- Nonexistent in bipolar technology, the zero offset property proves crucial in precise sampling of analog signals.

Ex. 12.3 Sampling speed considerations

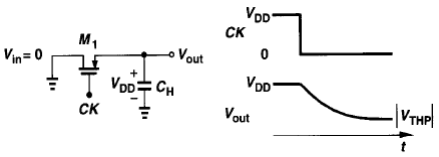


Figure 12.13 Sampling circuit using PMOS switch.

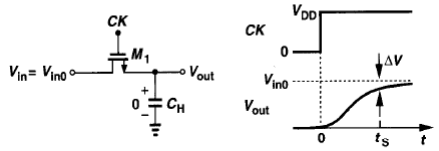


Figure 12.14 Definition of speed in a sampling circuit.

- Speed: Time from zero to maximum input level after the switch turns on, or more relevant: time to settle within a certain "error band", ΔV.
- Sampling speed is given by the on-resistance of the switch and the value of the sampling capacitor.
- R_{on} depends on input level, giving a greater time constant for more positive inputs (in the case of NMOS switches)

D/A (DAC) settling time and sampling rate

- In a DAC the settling time is defined as the time it takes for the converter to settle within some specified amount of the final value (usually 0.5 LSB).
- The sampling rate is the rate at which samples can be continously converted and is typically the inverse of the settling time.
- Different combinations of input vectors give different settling times. Picture from "High-speed data converters fully integrated in CMOS", dissertation for the dr. scient. degree by Leif Hanssen, Ifi, UiO, 1990.

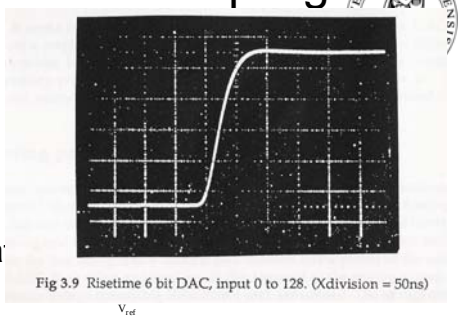
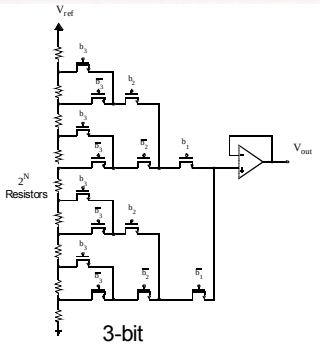


Fig 3.9 Risetime 6 bit DAC, input 0 to 128. (Xdivision = 50ns)



Ex. 12.3 Complimentary MOS switch

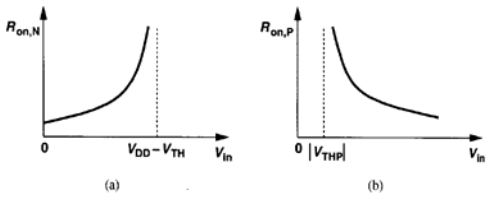


Figure 12.15 On-resistance of (a) NMOS and (b) PMOS devices as a function of input voltage.

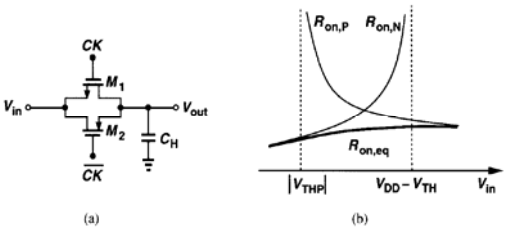


Figure 12.16 (a) Complementary switch, (b) on-resistance of the complementary switch.

- NMOS on resistance increases as the input voltage becomes more positive (and vice versa)
- PMOS on-resistance has the opposite behaviour and decreases as the input voltage becomes more positive.
- Combine PMOS and NMOS for complementary switches and rail-to-rail swings (, when needed).

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Complementary switches need complementary clocks

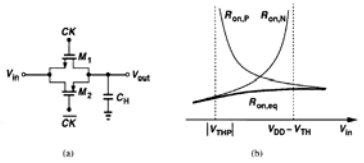

Figure 12.16 (a) Complementary switch, (b) on-resistance of the complementary switch.

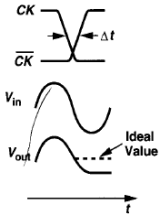

Figure 12.17 Distortion generated if complementary switches do not turn off simultaneously.

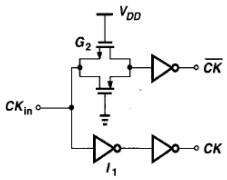

Figure 12.18 Simple circuit generating complementary clocks.

- The complementary switch reveals much less variation in on-resistance than that corresponding to each switch alone.
- For high-speed input signals the PMOS and NMOS switches must turn off simultaneously. (If for example the NMOS turns off Δt seconds earlier than the PMOS, the output voltage tends to track the input for the remaining Δt seconds, giving rise to distortion in the sampled value.)
- Fig. 12.18 shows a complementary clock generator for moderate precision.

A BiCMOS Sample-and-Hold for satellite communications

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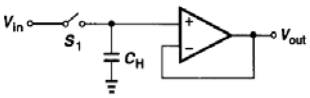
Summary

70 MHz is a very commonly used intermediate frequency (IF) in satellite communication systems. Direct conversion of this high frequency signal requires a very expensive ADC capable of operation at a clock rate twice this frequency. However, a narrow band 68 - 72 MHz can be folded down to 4 - 8 MHz with a sample-and-hold clocked at 16 MHz. Such undersampling allows conversion using a simple ADC with an accuracy of 6 - 8 bit. This ADC can be realized in CMOS with low area- and power consumption.

This configuration puts heavy requirements on the sample-and-hold. Two factors needing special attention are analog input bandwidth and aperture uncertainty (jitter). Other important specifications include total harmonic distortion (THD), signal-to-noise-plus-distortion ratio [S/(N+D)] and intermodulation distortion (IMD).

A traditional CMOS sample-and-hold contains an input MOSFET switch, a hold capacitor and an unity-gain output buffer. The high analog input frequency makes this an inadequate solution. The ON-resistance in the switch varies with the input level, resulting in variation in magnitude and phase, hence distortion. Limited slew rate on the switch gate voltage combined with a high dV/dt for the input signal also introduce aperture uncertainty (jitter).

BiCMOS offers the possibility of designing integrated circuits with speed-power-density performance previously unattainable with either technology individually. A BiCMOS sample-and-hold circuit has been made with a special attempt to overcome problems concerning the high analog input frequency. The input switch is implemented as a diode bridge using bipolar transistors. In sample mode this switch works as an input buffer.In hold mode the capacitor is buffered and held by a feedback loop containing two of the transistors in the diode bridge. The output buffer and the bias circuits have mainly been implemented with MOSFETs. A 1 bit current-steering DAC switches between the sample and hold modes. Turning current sinks on and off is then avoided, resulting in increased switching speed. With this configuration an input bandwidth of 100 MHz with a 2.5 pF hold capacitor has been obtained. Input voltage swing is limited to about 1.2 V_{P-P}. The circuit has been integrated in a 2 micron BiCMOS technology offered by Eurochip. The active area is 0.16 mm^2 and the circuit has a single +5V power supply. Power consumption has been calculated to less than 20 mW.



- 2 µm BiCMOS, 1993
- *"…A traditional CMOS Sample-and-Hold contains an input MOSFET switch, a hold capacitor and an unity-gain buffer. The high analog input frequency makes this an inadequate solution. The ON-resistance of the switch varies with the input level, resulting in variation in magnitude and phase, hence distortion. Limited slew rate on the switch gate voltage combined with a high dV/dt for the input signal also introduce aperture uncertainty (jitter)…"*

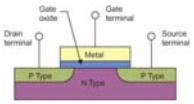
Charge injection due to channel capacitance

- When the clock signal goes low, the charge is distributed equally between the drain and source of M_1.
- is linearly related to V_{in}, resulting in a gain error for the S/H.
  There is also a linear relationship to V_{TH}, which is nonlinearly related to Vin (through Vsb) resulting in distortion for the overall S/H.
- Equal distribution (S/D) imprecise; worst-case: all charge to one node.

$$Q_{ch} = WLC_{ox}(V_{DD} - V_{in} - V_{TH}), \quad (12.28)$$

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H}. \quad (12.29)$$

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{C_H}, \quad (12.30)$$



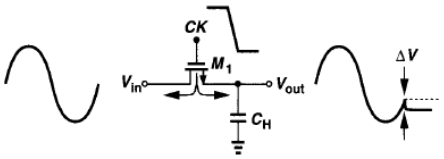


Figure 12.20 Effect of charge injection.

Charge injection leads to gain error, dc offsets and nonlinearity

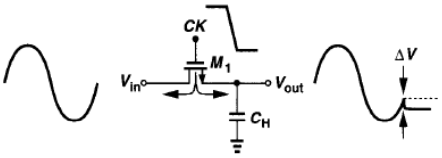


Figure 12.20 Effect of charge injection.

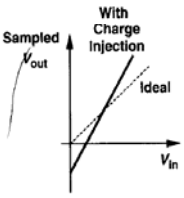


Figure 12.21 Input/output characteristic of sampling circuit in the presence of charge injection.

- In reality the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as impedance seen at each terminal to ground and the transition time of the clock. No good rule of thumb.
- Most circuit simulators model charge injection quite innacurately.
- The assumed linear function of the input voltage, leading to gain error and dc offset (only) is imprecise, due to nonlinear behaviour of V_{TH} upon V_{in}.

Clock feedthrough

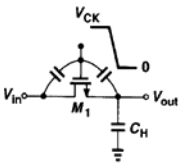
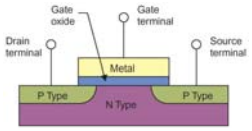


Figure 12.22 Clock feedthrough in a sampling circuit.



$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov}+C_H},$$

- Clock transitions are coupled through gate-drain and gate-source overlap capacitances.
- The error, ΔV, is independent of the input level, manifesting itself as a constant offset in the input/output characteristic.

19

kT/C noise

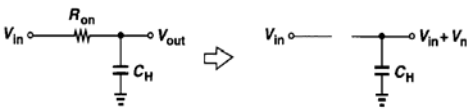


Figure 12.23 Thermal noise in a sampling circuit.

value of the input voltage. It can be proved that the rms voltage of the sampled noise in this case is still approximately equal to $\sqrt{kT/C}$ [3, 4].

- A resistor charging a capacitor gives rise to a total rms noise voltage of SQRT (kT/C).
- The noise gets stored on the capacitor along with the instantaneous value of the input voltage.
- In order to achieve low noise the sampling capacitor must be sufficiently large, thus loading other circuits and degrading the speed.

20

Charge injection cancellation

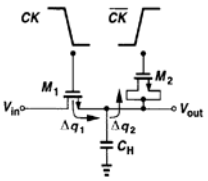


Figure 12.24 Addition of dummy device to reduce charge injection and clock feedthrough.

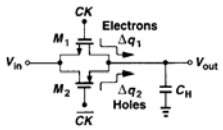


Figure 12.26 Use of complementary switches to reduce charge injection.

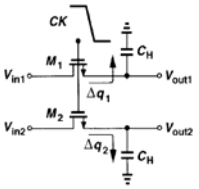


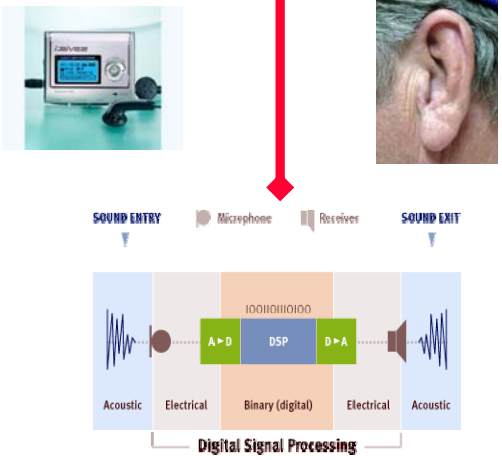
Figure 12.27 Differential sampling circuit.

Fig. 12.24: The deposited channel charge is absorbed by the latter.

Dimension W2 = 0.5W1 and L1 = L2. But: The approach is not very attractive as the underlying assumption of equal splitting between S and D is generally invalid.

- Fig. 12.26: Attempts to match dimensions leads to cancellation for only one input level.
- Better: differential operation (Fig. 12.27) Charge inj. Is common mode disturbance. Nonlinearity of body effect leads to odd order distortion.
- Charge injection limits the speed precision envelope in sampled-data systems

Data Converter Fundamentals (chapter 11)



Some systems exploiting data converters, "Allen & Holberg"

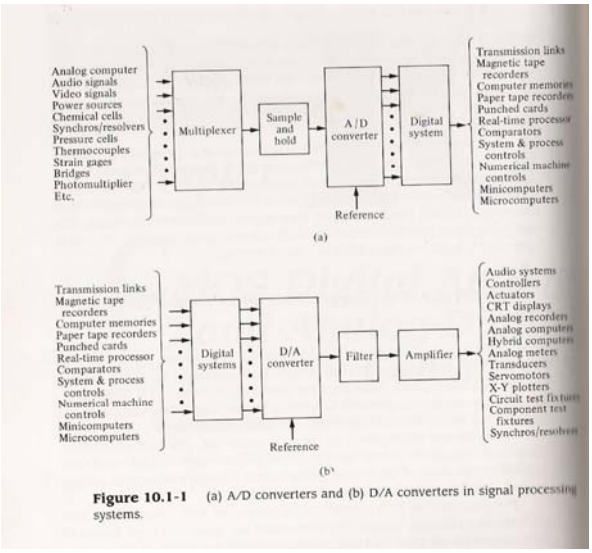


Figure 10.1-1 (a) A/D converters and (b) D/A converters in signal processing systems.

Different ADCs depending on needs

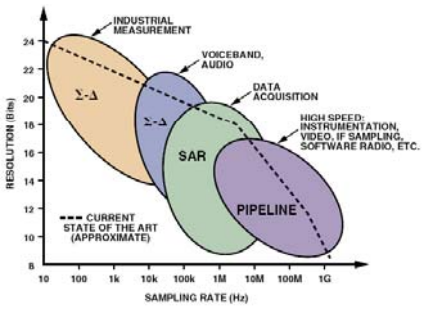


Figure 1. ADC architectures, applications, resolution, and sampling rates.

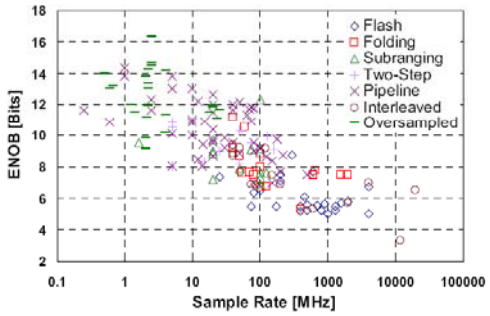


Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

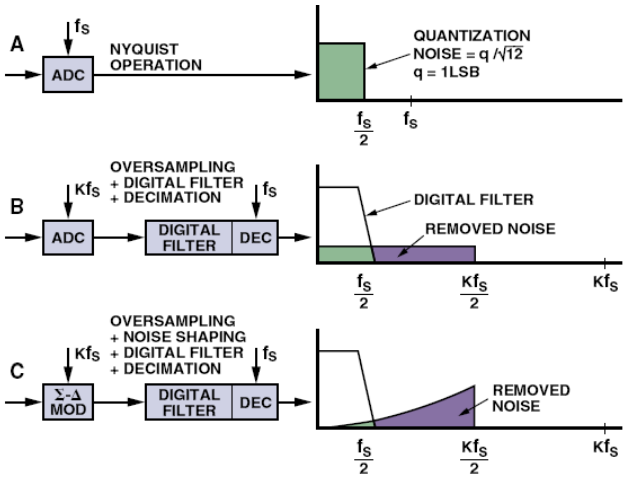
Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]
[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

Main data converter types:

- Nyquist-rate converters:
  - Each value has a one-to-one correspondencewith a single input
  - The sample-rate must be at least equal to twice the signal frequency (Typically somewhat higher)
- Oversampled converters:
  - The sample-rate is much higher than the signal frequency, typically 20 – 512 times.
  - The extra samples are used to increase the SNR
  - Often combined with noise shaping

Nyquist Sampling, Oversampling, Noise Shaping



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

Flash ADC from 1926 (Analog Digital Conversion handbook, Analog Devices)

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5—see further discussions in Chapter 1 of this book). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection (see Figure 3.49). Each individual photocell output activates part of a relay network which generates the 5-bit binary code.

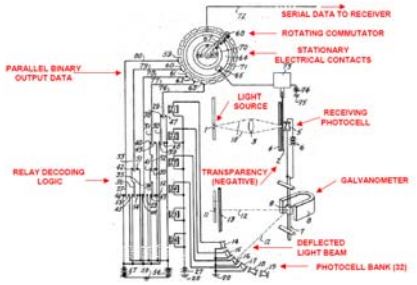
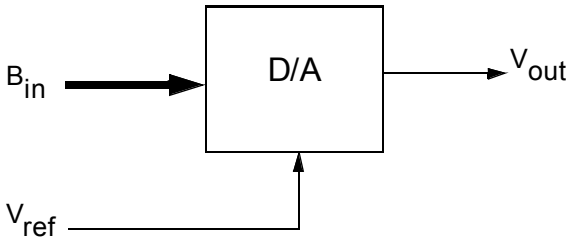


Figure 3.49: *A 5-Bit Flash ADC Proposed by Paul Rainey*
Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926

Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

Example : 8-bit D/A converter

An ideal D/A converter has

$$V_{ref} = 5\ V$$

Find Vout when

$$B_{in} = 10110100$$

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0{,}703125$$

$$V_{out} = V_{ref} B_{in} = 3{,}516\ V$$

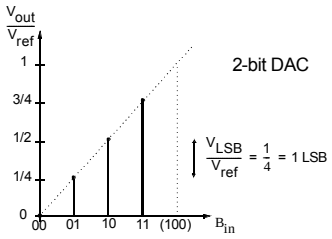
Find

$$V_{LSB}$$

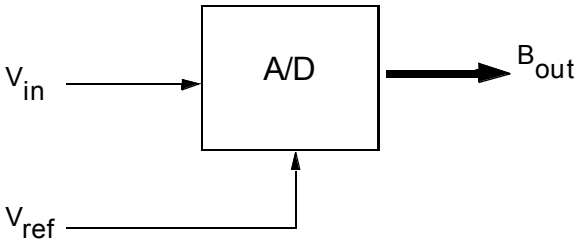
$$V_{LSB} = 5/256 = 19{,}5\ mV$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

$$1\ LSB = \frac{1}{2^N}$$



Ideal A/D converter (Fig. 11.3)

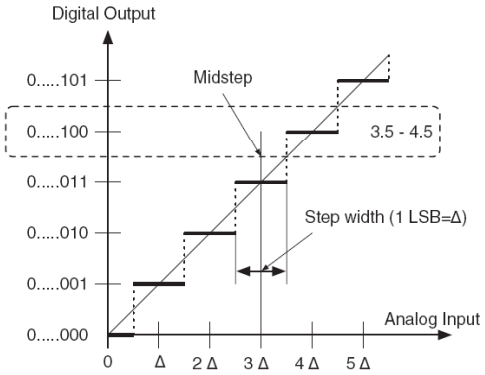


$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm V_x$$

where

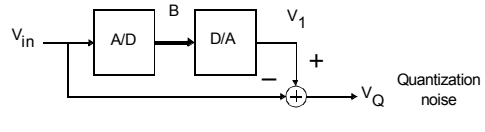
$$-\frac{1}{2}V_{LSB} \le V_x < \frac{1}{2}V_{LSB}$$

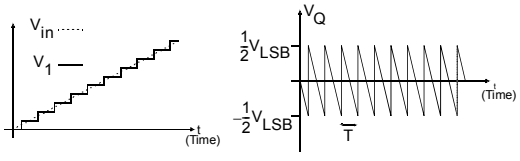
Ideal transfer curve for a 2-bit A/D converter (Fig. 2.2)



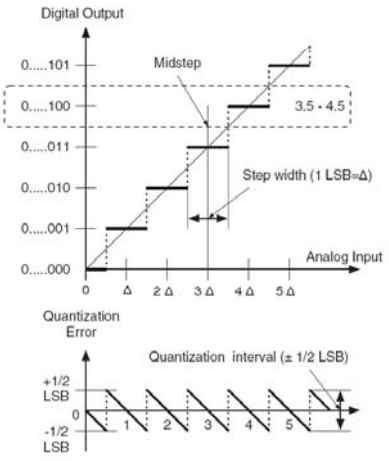
- A range of input values produce the same output value (QA range of input values produce the same output value (Quantization error)
- Different from the D/A case

Quantization noise ("J&M" + "M")

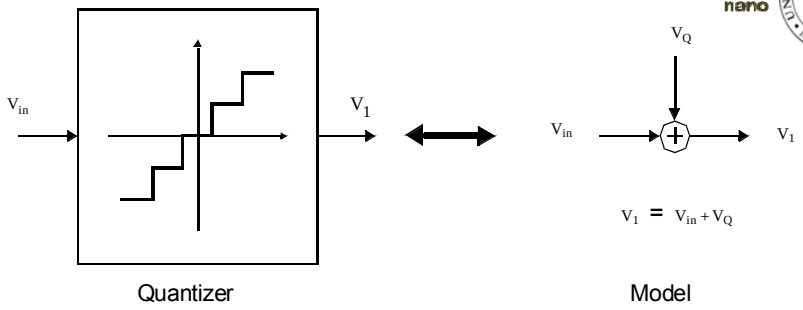




$$V_Q = V_1 - V_{in}$$



Quantization noise model



•TThe model is exact as long as Vq is properly defined

•Vq is most often assumed to be white and uniformely distributed between +/- Vlsb/2

Quantization noise

•The rms-value of the quantization noise can be shown to be:

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}}$$

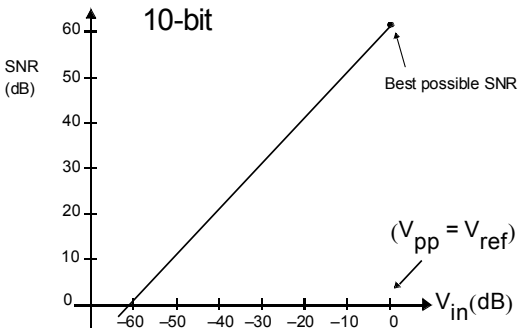
•Total noise power is independent of sampling frequency

•In the case of a sinusoidal input signal with p-p amplitude of $V_{ref}/2$

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right)$$

$$SNR = 6{,}02N + 1{,}76\ \text{dB}$$

Quantization noise



•Signal-to Noise ratio is highest for maximum input signal amplitude

Signed codes

Table 11.1 Some 4-bit signed digital representations

Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(–0)	(–0)	(1000)	(1111)		
–1	–1/8	1001	1110	0111	1111
–2	–2/8	1010	1101	0110	1110
–3	–3/8	1011	1100	0101	1101
–4	–4/8	1100	1011	0100	1100
–5	–5/8	1101	1010	0011	1011
–6	–6/8	1110	1001	0010	1010
–7	–7/8	1111	1000	0001	1001
–8	–8/8			0000	1000

- Unipolar / bipolar
- Common signed digital repr.: sign magnitude, 1's complement, 2's compl.
- Sign. M.: 5:0101, -5:1101, two repr. Of 0, 2^N-1 numb.
- 1's compl.: Neg. Numbers are complement of all bits for equiv. Pos. Number: 5:0101, -5:1010
- Offset bin: 0000 to the most neg., and then counting up..

  +: closely related to unipolar through simple offset

2's complement

A3a2a1a0	Sign magnitude	2s complement
0111	+7	+7
0110	+6	+6
0101	+5	+5
0100	+4	+4
0011	+3	+3
0010	+2	+2
0001	+1	+1
0000	+0	+0
1000	-0	-8
1001	-1	-7
1010	-2	-6
1011	-3	-5
1100	-4	-4
1101	-5	-3
1110	-6	-2
1111	-7	-1

- 5_{10} : 0101 = $2^2 + 2^0$
- - 5_{10} : (0101)' +1 = 1010 + 1 = 1011

- Addition of positive and negative numbers is straightforward, using addition, and requires little hardware
- 2's complement is most popular representation for signed numbers when arithmetic operations have to be performed

7_{10}-6_{10} via addition using two's complement of -6

- 0000 0000 0000 0000 0000 0000 0000 0000 $00111_2 = 7_{10}$
- 0000 0000 0000 0000 0000 0000 0000 0000 $00110_2 = 6_{10}$
- *Subtraction uses addition: The appropriate operand is negated before being added*
- *Negating a two's complement number: Simply invert every 0 and 1 and add one to the result.* Example:
- 0000 0000 0000 0000 0000 0000 0000 0000 0110_2 becomes
- 1111 1111 1111 1111 1111 1111 1111 1111 1001_2

\+ 1_2

= 1111 1111 1111 1111 1111 1111 1111 1111 1010_2

0000 0000 0000 0000 0000 0000 0000 0000 $0111_2 = 7_{10}$

\+ 1111 1111 1111 1111 1111 1111 1111 1111 $1010_2 = -6_{10}$

= 0000 0000 0000 0000 0000 0000 0000 0000 $0001_2 = 1_{10}$

performance limitations

- Resolution
- Offset and gain error
- Accuracy
- Integral nonlinearity (INL) error
- Differential nonlinearity (DNL) error
- Monotonicity
- Missing codes
- A/D conversion time and sampling rate
- D/A settling time and sampling rate
- Sampling time uncertainty
- Dynamic range
- NB!! Different meanings and definitions of performance parameters sometimes exist. → Be sure what's meant in a particular specification or scientific paper.. There are also more than those mentioned here.

Resolution

- Resolution usually refers to the number of bits in the input (D/A) or output (ADC) word, and is often different from the accuracy.
- Analog-Digital Conversion Handbook, Analog Devices, 3rd Edition, 1986: *An n-bit binary converter should be able to provide 2n distinct and different analog output values corresponding to the set of n binary words. A converter that satisfies this criterion is said to have a resolution of n bits.*

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

TABLE I
KEY DATA FOR THE ADC

Nominal sampling rate	110MS/s
Technology	0.18μm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{p-p}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

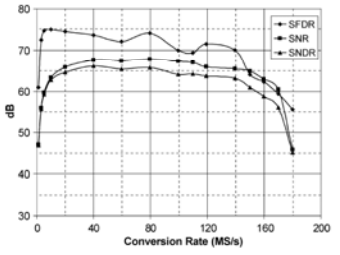


Fig. 8. SFDR, SNR, and SNDR versus conversion rate. The input frequency and signal swing is 10 MHz and 2V $_{p-p}$, respectively.

Litterature

- Johns & Martin: ”Analog Integrated Circuit Design”
- Franco Maloberti: ”Data Converters”

41

Next week:

- Data converter fundamentals, among them some principles especially relevant for your project.
- Messages are given on the INF4420 homepage.
- Questions: sa@ifi.uio.no , 22852703 / 90013264

Transistor stuff.

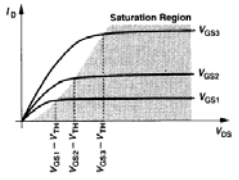


Figure 2.15 Saturation of drain current.

Writing

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (2.29)$$

and $\lambda \propto 1/L$, we note that if the length is doubled, the slope of I_D vs. V_{DS} is divided by *four* because $\partial I_D/\partial V_{DS} \propto \lambda/L \propto 1/L^2$ (Fig. 2.26). For a given gate-source overdrive, a larger L gives a more

Figure 2.26 Effect of doubling channel length.

Figure 2.12 Linear operation in deep triode region.

Figure 2.13 MOSFET as a controlled linear resistor.

current. With the condition $V_{DS} \ll 2(V_{GS} - V_{TH})$, we say the device operates in deep triode region.

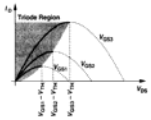


Figure 2.11 Drain current versus drain-source voltage in the triode region.

Fig. 2.11 plots the parabolas given by (2.8) for different values of V_{GS}, indicating that the "current capability" of the device increases with V_{GS}. Calculating $\partial I_D/\partial V_{DS}$, the reader can show that the peak of each parabola occurs at $V_{DS} = V_{GS} - V_{TH}$ and the peak current is

$$I_{D,max} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2. \quad (2.9)$$

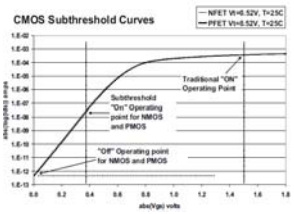
We call $V_{GS} - V_{TH}$ the "overdrive voltage"[4] and W/L the "aspect ratio." If $V_{DS} \leq V_{GS} - V_{TH}$, we say the device operates in the "triode region."[5]

If in (2.8), $V_{DS} \ll 2(V_{GS} - V_{TH})$, we have

$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS}, \quad (2.10)$$

that is, the drain current is a *linear* function of V_{DS}. This is also evident from the characteristics of Fig. 2.11 for small V_{DS}; as shown in Fig. 2.12, each parabola can be approximated by a straight line. The linear relationship implies that the path from the source to the drain can be represented by a linear resistor equal to

$$R_{on} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})}. \quad (2.11)$$



- Saturation.. Vgs ≥ Vth. Vds sufficiently high so that Vgd < Vth; Vds ≥ (Vgs – Vth)

Triode: Vgs ≥Vth, Vds sufficiently high so Vgd < Vth

- Cutoff / subthreshold: Vgs < Vth