Oversampling Data Converters

Tuesday, March 15th, 9:15 – 11:40

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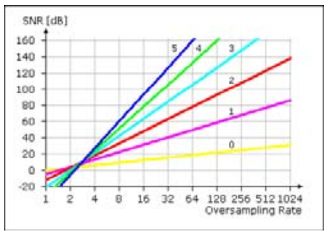
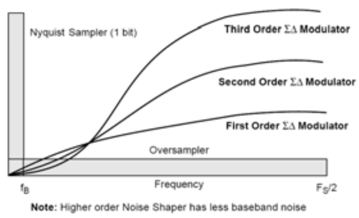
Last time – and today, Tuesday 15th of March:

Last time:

12.3 Switched Capacitor Amplifiers
12.4 Switched Capacitor Integrator

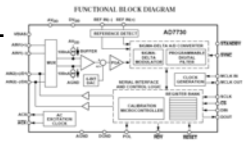
Today, from chapter 14 in "J. & M.":
14.1 Oversampling without noise shaping
14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
2nd order sigma delta design example



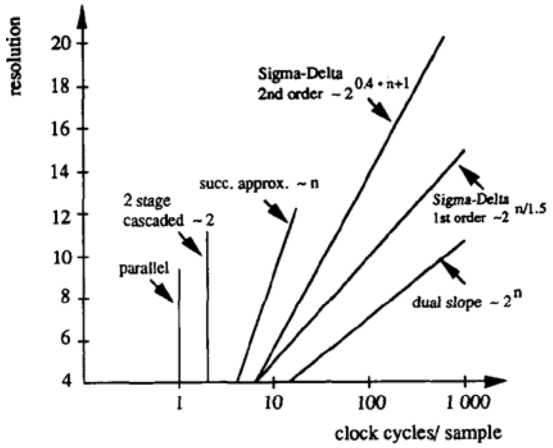


Oversampling converters (chapter 14 in "J & M")

- For high resolution, low-to-medium-speed applications like for example digital audio
- Relaxes requirements placed on analog circuitry, including matching tolerances and amplifier gains
- Simplify requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A converters.
- Sample-and-Hold is usually not required on the input
- Extra bits of resolution can be extracted from converters that samples much faster than the Nyquist-rate. Extra resolution can be obtained with lower oversampling rates by exploiting noise shaping



Resolution and clock cycles per sample



. Dependence of achievable resolution and required clock cycles per sample for various ADC systems.

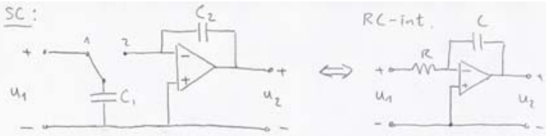
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 27, NO. 10, OCTOBER 1992

A Gigasample/Second 5-b ADC with On-Chip Track and Hold Based on an Industrial 1-μm GaAs MESFET E/D Process

Richard Hagelauer, *Member, IEEE*, Frank Oehler, Günter Rohmer, Josef Sauerer, and Dieter Seitzer, *Senior Member, IEEE*

Transfer function for simple discrete time integrator

SC:



$\boxed{Q = C \cdot V}$

$f = \frac{1}{T}$

Svitsjen er ved tidspunkt $t = (n-1)T$ i posisjon 1, og det blir tatt en punktprøve ("et sampel") av $u_1(t)$, da C_1 blir ladet til:

$$q_1[(n-1)T] = C_1 \cdot u_1[(n-1)T]$$

Ladningen på C_2 er (samtidig):

$$q_2[(n-1)T] = C_2 \cdot u_2[(n-1)T]$$

Ved tidspunkt $t = n \cdot T$ blir ladningen på C_1 overført til C_2 ved at svitsjen er i posisjon 2.
Hele ladningen på C_1 blir ført over til C_2 fordi operasjonsforst. tvinger spenningen over C_1 til å bli null.

Ladn. på C_1 subtraheres dermed fra ladn. på C_2.

ref.: Nils Haaheim: "Analog CMOS", Universitetet i Trondheim - NTH, 1994

Ladn. på C_2 ved $t = nT$ blir dermed:

$$q_2[nT] = q_2[(n-1)T] - q_1[(n-1)T]$$

$$\Updownarrow$$

$$C_2 \cdot u_2[nT] = C_2 \cdot u_2[(n-1)T] - C_1 u_1[(n-1)T]$$

$$\Updownarrow$$

$$u_2[nT] = u_2[(n-1)T] - \frac{C_1}{C_2} \cdot u_1[(n-1)T]$$

Kan benytte z-transform

OBS! If $x(n) \leftrightarrow X(n)$, then $x(n-k) \leftrightarrow z^{-k} X(z)$

$$U_2(z) = U_2(z) \cdot z^{-1} - \frac{C_1}{C_2} U_1(z) z^{-1}$$

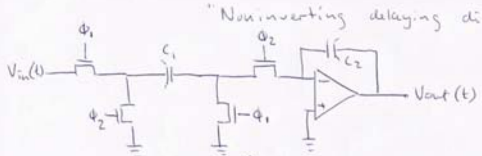
$$\Updownarrow$$

$$H(z) = \frac{U_2(z)}{U_1(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{(1 - z^{-1})}$$

-

Transfer function not dependent on Cp1: (Circuit in Fig. 10.9)

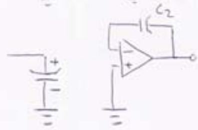
"Noninverting delaying discrete-time int." ("J&M" p. 405)



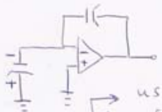
$\boxed{Q = C \cdot V}$

Remember, from chapter 9:
If $x(n) \leftrightarrow X(z)$ then $x(n-k) \leftrightarrow z^{-k} X(z)$

Φ_1:



Φ_2:



At time $t = (n-1)T$, in Φ_1, a "sample" of the input voltage is taken, and C_1 gets charged:

$$q_{C1}[(n-1)T] = C_1 \cdot v_{in}[(n-1)T]$$

At the same time, there is a charge on C_2:

$$q_{C2}[(n-1)T] = C_2 \cdot v_{out}[(n-1)T]$$

At time $t = nT$ the charge on C_1 is transmitted to C_2:

$$q_{C2}[nT] = q_{C2}[(n-1)T] + q_{C1}[(n-1)T]$$

using $Q = C \cdot V$:

$$C_2 \cdot v_{out}[nT] = C_2 \cdot v_{out}[(n-1)T] + C_1 v_{in}[(n-1)T]$$

$$\Updownarrow \quad \text{z-transf.:}$$

$$C_2 V_{out}(z) = C_2 V_{out}(z) \cdot z^{-1} + C_1 V_{in}(z) \cdot z^{-1}$$

$$\Updownarrow$$

$$C_2 V_{out}(z) - C_2 V_{out}(z) \cdot z^{-1} = C_1 V_{in}(z) \cdot z^{-1}$$

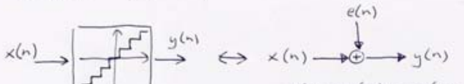
$$\Updownarrow$$

$$C_2 V_{out}(z)(1 - z^{-1}) = C_1 V_{in}(z) \cdot z^{-1}$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}}$$

QUANTIZATION NOISE (p. 532 - 533 in "J & M")

The quantization noise is the difference between the input and output values.



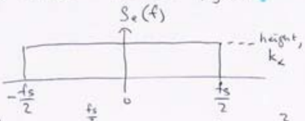
$e(n) = y(n) - x(n)$

This model is exact under the assumption that the quantization error is strongly related to the input signal ("J & M" p. 532) The model becomes approximate when assumptions are made about the statistical properties of e(n), such as e(n) being an independent white-noise signal. This model leads to a simpler understanding of ΣΔ and with some exceptions is usually reasonably accurate.

- If x(n) is very active, e(n) can be approximated as an independent random number uniformly distributed between $\pm\frac{\Delta}{2}$, where Δ equals the difference between two adjacent quantization levels.

Thus, the quantization noise power equals $\frac{\Delta^2}{12}$ (Sec. 11.3) and is independent of the sampling frequency, f_s

The spectral density of e(n), $S_e(f)$ is white (constant over freq.) and all its power within $\pm f_s/2$, as shown in the figure:



$$\int_{-f_s/2}^{f_s/2} S_e^2(f)\,df = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} k_x^2\,df = (k_x)^2 \cdot f_s = \frac{\Delta^2}{12}$$

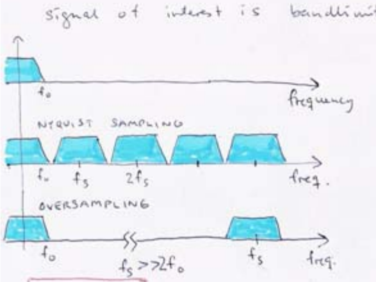
$$\Updownarrow$$

$$k_x = \frac{\Delta}{\sqrt{12}}\sqrt{\frac{1}{f_s}}$$

The spectral density height is calculated by noting that the total noise power is $\Delta^2/12$ and with a two-sided def. of power equals the area under $S_e(f)$ within $+/- f_s/2$

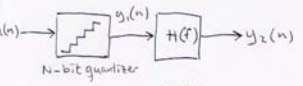
OVERSAMPLING ADVANTAGE p. 535

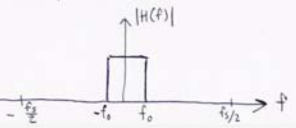
signal of interest is bandlimited to f_0



$$\boxed{OSR \equiv \frac{f_s}{2f_0}}$$

After quantization, $y_1(n)$ is filtered by H(f) to create $y_2(n)$ that eliminates quantization noise (together with any other signals) greater than f_0.





If the input is sinusoidal, its maximum peak value without clipping is $2^N(\Delta/2)$

For this wave the signal power, P_s, has a power equal to $P_s = \left(\frac{\Delta 2^N}{2}\frac{1}{\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$

The power of the input signal within $y_2(n)$ remains the same as before since we assumed the signal's frequency content is below f_0.

HOWEVER, THE QUANTIZATION NOISE POWER IS REDUCED TO

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\,|H(f)|^2\,df = \int_{-f_0}^{f_0} k_x^2\,df$$

$$= \frac{2f_0}{f_s}\cdot\frac{\Delta^2}{12} = \frac{\Delta^2}{12}\left[\frac{1}{OSR}\right]$$

> THEREFORE, DOUBLING OSR DECREASES THE QUANTIZATION NOISE POWER BY ONE-HALF, OR EQUIVALENTLY, 3 dB (or equiv. 0.5 bits)

$$SNR_{MAX} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR)$$

$$= \underbrace{6.02N + 1.76}_{\text{due to N-bit quantizer}} + \underbrace{10\log(OSR)}_{\text{due to oversampling}}\ [dB]$$

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) \wedge P_s = \frac{\Delta^2 2^{2N}}{8} \wedge P_e = \frac{\Delta^2}{12}\frac{1}{OSR}$$

$$\Downarrow$$

$$SNR_{max} = 10 \log\left[\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}\cdot\frac{1}{OSR}}\right] = 10 \log\left[\frac{\frac{\Delta^2 \cdot 2^{2N}}{2\cdot 2\cdot 2}}{\frac{\Delta^2}{2\cdot 2\cdot 3}\frac{1}{OSR}}\right] = 10 \log \frac{3}{2} 2^{2N} \cdot OSR$$

$$= 10 \log \frac{3}{2} \cdot 2^{2N} + 10 \log OSR$$

$$= 10 \log \frac{3}{2} + 10 \log 2^{2N} + 10 \log OSR$$

$$= 10 \log 2^{2N} + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2N \cdot \log 2 + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2 \cdot N \cdot 0.301 + 1.76 + 10 \log OSR$$

$$= 6.02N + 1.76 + 10 \log(OSR) \quad [dB]$$

$\log_b(c^p) = p\log_b(c$

$\log(xy) = \log x + \log y$

(14.13) pp. 536 i J&M.

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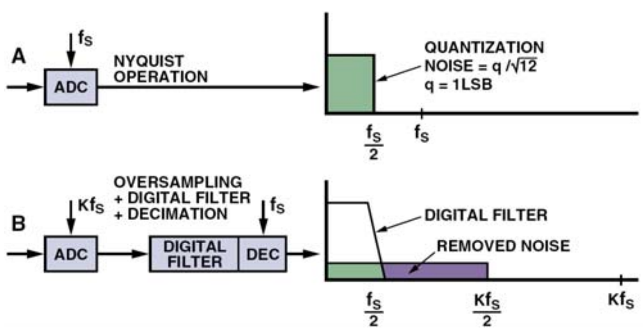
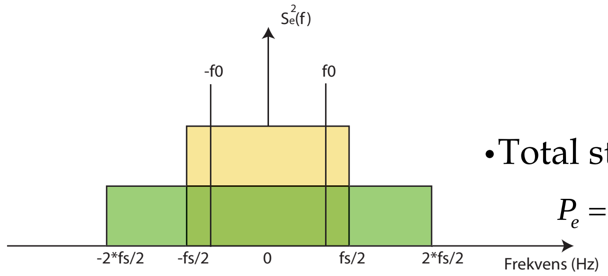
Nyquist Sampling and Oversampling



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

Oversampling (without noise shaping)

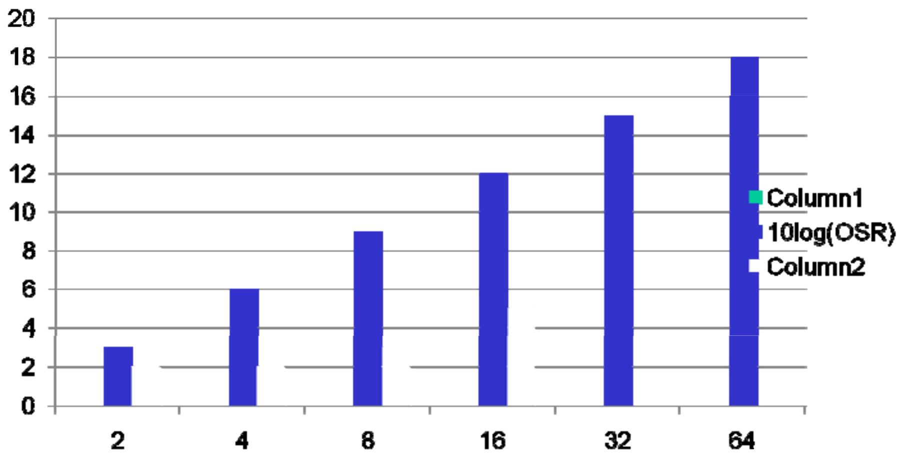


- Total støy er gitt av:

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)df = \frac{\Delta^2}{12} \cdot \frac{1}{OSR}$$

- Doubling of the sampling frequency increases the dynamic range by 3 dB = 0.5 bit.
- To get a high SNR a very high fs is needed → high power consumption.
- Oversampling usually combined with noise shaping and higher order modulators, for higher increase in dynamic range per octave ("OSR")

SNRmax = 6.02N+1.76+10log(OSR) [dB]
SNR improvement 0.5 bits / octave



Ex. 14.3

EXAMPLE 14.3

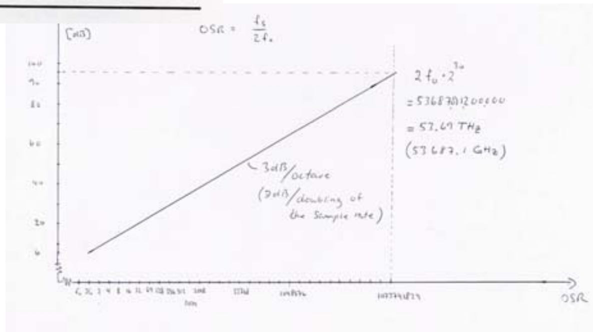
Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0 = 25$ kHz ? (Note that the input into the A/D converter has to be very active for the white-noise quantization model to be valid—a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping).

Solution

Oversampling (without noise shaping) gives 3 dB/octave where 1 octave implies doubling the sampling rate. We require 90 dB divided by 3 dB/octave, or 30 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{30} \times 2f_0 \cong 54{,}000 \text{ GHz !}$$

This example shows why noise shaping is needed to improve the SNR faster than 3 dB/octave, since 54,000 GHz is highly impractical.



Advantages of 1-bit A/D converters (p.537 in "J&M")

- Oversampling improves signal-to-noise ratio, but not linearity
- Ex.: 12-bit converter with oversampling needs component accuracy to match better than 16-bit accuracy if a 16-bit linear converter is desired
- Advantage of 1-bit D/A is that it is inherently linear. Two points define a straight line, so no laser trimming or calibration is required
- Many audio converters presently use 1-bit converters for realizing 16- to 18-bit linear converters (with noise shaping).

Oversampling with noise shaping (14.2)

- Oversampling combined with noise shaping can give much more dramatic improvement in dynamic range each time the sampling frequency is doubled.
- The sigma delta modulator converts the analog signal into a noise-shaped low-resolution digital signal.
- The decimator converts to a high resolution digital signal

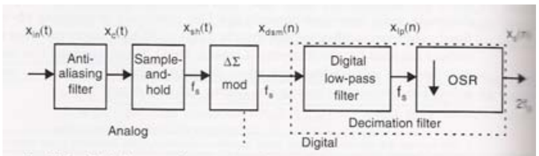
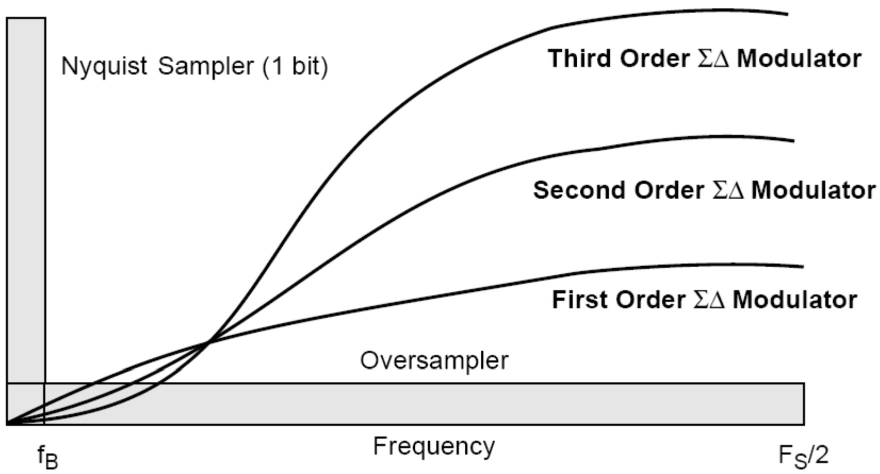


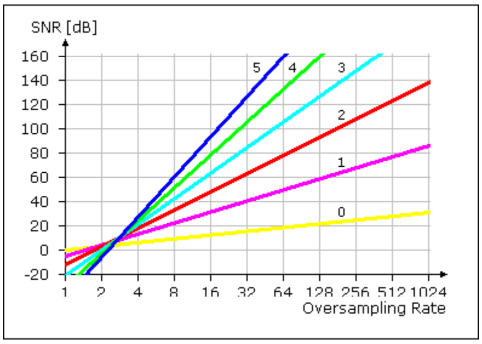
Fig. 14.5 Block diagram of an oversampling A/D converter.

Multi-order sigma delta noise shapers (Sangil Park, Motorola)



Note: Higher order Noise Shaper has less baseband noise

Ex. 14.5 "point":

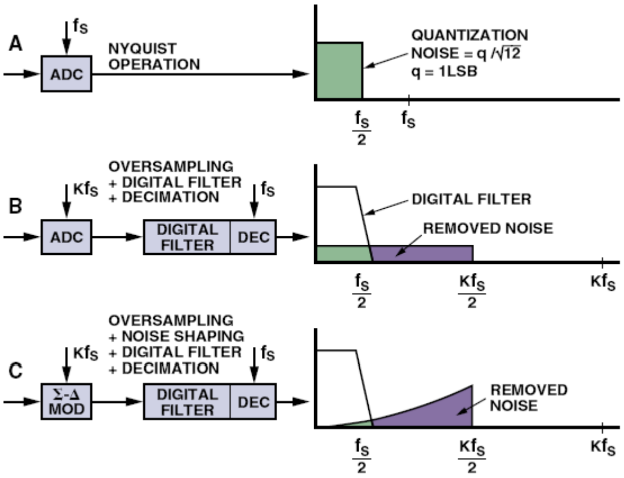


- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- 6 db Quantizer, for 96 dB SNR:
- Plain oversampling: f_s=54 GHz
- 1st order : f_s=75.48 MHz
- 2nd order: f_s= 5.81 MHz

3 a) (Weight 10 %)

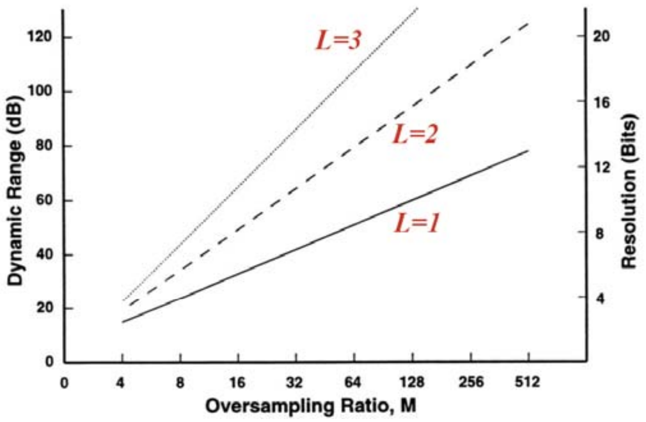
A sampled signal is bandlimited to f_0 = 22 kHz.What is the sampling frequency, f_s, for an oversampling ratio ("OSR") of 128?
A 1-bit analog-to-digital converter ("ADC") has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used?
What is the maximum SNR in the similar case exploiting 2nd order noise shaping?
If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

Nyquist Sampling, Oversampling, Noise Shaping



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

OSR, modulator order and Dynamic Range



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- Oversampling and noise shaping

14.2 Oversampling with noise shaping

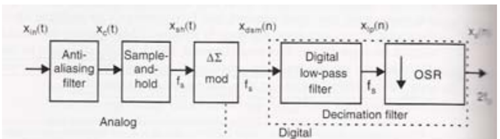
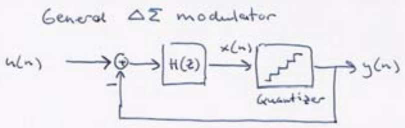


Fig. 14.5 Block diagram of an oversampling A/D converter.

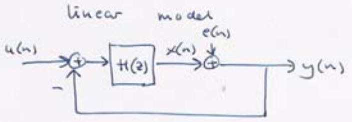
- The anti aliasing filter bandlimits the input signals less than $f_s/2$.
- The continous time signal $x_c(t)$ is sampled by a S/H (not necessary with separate S/H in Switched Capacitor impl.)
- The Delta Sigma modulator converts the analog signal to a noise shaped low resolution digital signal
- The decimator converts the oversampled low resolution digital signal into a high resolution digital signal at a lower sampling rate usually equal to twice the desired bandwidth of the desired input signal (conceptually a low-pass filter followed by a downsampler).

Noise shaped Delta Sigma Modulator

General ΔΣ modulator

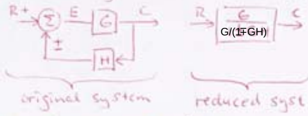


linear model

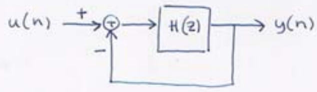


The linear model can be treated as having two independent inputs (which is an approximation).

BLOCK DIAGRAM ALGEBRA Cathey & Nasar p. 292; eliminating a feedback loop:



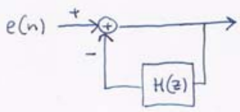
Signal :



Signal transfer function, $S_{TF}(z)$:

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}$$

Noise :



Noise transfer function, $N_{TF}(z)$:

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

The output is the combination of the input and noise: $Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z)$

First-Order Noise Shaping (Figures from Schreier & Temes '05)

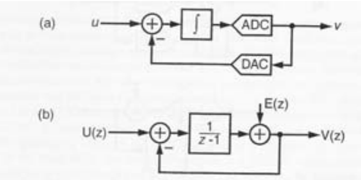


Figure 1.4: (a) A delta-sigma modulator used as an ADC and (b) its linear z-domain model.

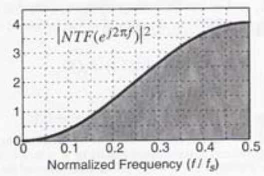


Figure 1.5: Noise-shaping function for the ΔΣ modulator shown in Fig. 1.4.

- $S_{TF}(z)$ = [H(z)/1+H(z)] (eq. 14.15) $N_{TF}(z)$ = [1/1+H(z)]
- $Y(z) = S_{TF}(z)\,U(z) + N_{TF}(z)\,E(z)$
- H(z) = 1/z-1 (discrete time integrator) gives 1st order noise shaping
- $S_{TF}(z)$ = [H(z)/1+H(z)] = 1/(z-1)/[1+1/(z-1)] = z^{-1}
- $N_{TF}(z)$ = [1/1+H(z)] = 1/[1+1/(z-1)] = (1 – z^{-1})
- The signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator (i.e. a high-pass filter)

14.2 Oversampling with noise shaping

$$N_{TF}(f) = 1 - e^{-j2\pi f/f_s} = \left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right) \cdot e^{-j\pi f/f_s} = \frac{\left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right) \cdot 2j \cdot e^{-j\pi f/f_s}}{2j}$$

$$= \sin\left(\frac{\pi f}{f_s}\right) \cdot 2j \cdot e^{-j\pi f/f_s}$$

$$\boxed{\cos z = \frac{e^{jz} + e^{-jz}}{2} \qquad \sin z = \frac{e^{jz} - e^{-jz}}{2j}}$$

$$|N_{TF}(f)| = 2 \sin\left(\frac{\pi f}{f_s}\right) \quad (\text{"high-pass"})$$

Quantization noise power over the frequency band 0 to f_0 is now given by

$$P_e = \int_{-f_0}^{f_0} S_e^2(f) \cdot |N_{TF}|^2 \, df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_s} \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad (14.23)$$

Making the approximation that $f_0 << f_s$ ($OSR >> 1$) so that $\sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s}$:

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR}\right)^3, \quad OSR = \frac{f_s}{2f_0}$$

It is assumed that the maximum signal power is the same as obtained before, in equation 14.11 ($P_s = \Delta^2 2^{2N}/8$), making maximum SNR:

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} \cdot 2^{2N}\right) + 10 \log\left[\frac{3}{\pi^2} (OSR)^3\right], \text{ or:}$$

$$\boxed{SNR_{max} = 6.02N + 1.76 - 5.17 + 30 \log(OSR)}$$

Doubling the OSR gives an SNR improvement for a 1st order modulator of 9 dB/octave or, equiv. 1.5 bits/octave.

Quantization noise power for linearized model of a general ΔΣ modulator

$$P_e = \int_{-f_0}^{f_0} S_e^2(f) |N_{TF}(f)|^2 df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_s} \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad (14.23)$$

Using the approximation that $f_0 << f_s$ (i.e. $OSR >> 1$) so that we may approximate $\sin \frac{\pi f}{f_s}$ to be $\frac{\pi f}{f_s}$:

$$P_e = \int_{-f_0}^{f_0} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2 \frac{\pi f}{f_s}\right]^2 df = \int_{-f_0}^{f_0} \frac{\Delta^2}{12} \frac{1}{f_s} \frac{4\pi^2}{f_s^2} \cdot f^2 \, df$$

Letting $K = \frac{\Delta^2}{12} \frac{1}{f_s} \frac{4\pi^2}{f_s^2}$

$$P_e = K \int_{-f_0}^{f_0} f^2 \, df = \frac{K}{3}\left(f_0^3 - (-f_0)^3\right) = \frac{K}{3} \cdot 2 f_0^3$$

$$= \frac{\Delta^2}{12} \frac{1}{f_s} \frac{4\pi^2}{f_s^2 \cdot 3} \cdot f_0^3 = \frac{\Delta^2}{12} \frac{\pi^2}{3} \cdot \frac{2 \cdot 2 \cdot 2}{f_s^3} f_0^3 = \frac{\Delta^2}{12} \frac{\pi^2}{3} \left(\frac{2f_0}{f_s}\right)^3$$

Using $\boxed{OSR = \frac{f_s}{2f_0}} \Leftrightarrow \frac{2f_0}{f_s} = \frac{1}{OSR}$: $\quad P_e = \frac{\Delta^2 \pi^2}{36} \left(\frac{1}{OSR}\right)^3 \qquad (14.24)$

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Second-order noise shaping

Fig. 14.10 2nd order modulator

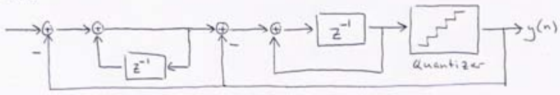
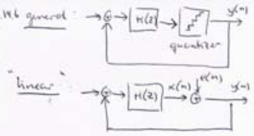


fig. 14.6 general:



The above modulator realizes 2nd order noise shaping.
The signal transfer function is given by

$$S_{TF}(f) = z^{-1}$$

The noise transfer function is given by

$$N_{TF}(f) = (1 - z^{-1})^2$$

Magnitude: $|N_{TF}(f)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2$

The quantization noise power over the frequency band of interest: $P_e \cong \frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5$

Max SNR:

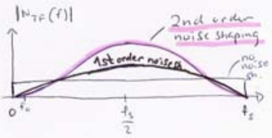
$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} 2^{2N}\right) + 10 \log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

or:

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \quad (14.32)$$

Doubling the OSR improves the SNR for a 2nd order mod. by 15dB.

fig. 14.11:



Ex. 14.5 p. 545:
1-bit A/D, 6-bit SNR. f_0 = 25 kHz
96 dB SNR is the goal.
Sample rate needed?
- oversampling: 54 THz
- 1st order n.s.: 75 MHz
- 2nd order n.s.: 5.8 MHz

Ex. 14.5

- Given that a 1-bit A/D converter has a 6 dB SNR, which sample rate is required to obtain a 96-dB SNR (or 16 bits) if f_0 = 25 kHz for straight oversampling as well as first-and second-order noise shaping?

- Oversampling with no noise shaping: From ex. 14.3 we know that straight oversampling requires a sampling rate of 54 THz.
- (6.02N+1.76+10 log (OSR) = 96
  <->
  6 + 10 log OSR = 96)

<-> 10 log OSR = 90

Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \quad (14.2$$

We see here that doubling the OSR gives an SNR improvement for a first-order modulator of 9 dB or, equivalently, a gain of 1.5 bits/octave. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

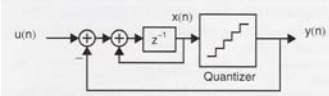


Fig. 14.7 A first-order noise-shaped interpolative modulator.

- Oversampling with 1st order noise shaping:
- 6 - 5.17 + 30 log(OSR) = 96 $\qquad$ OSR = f_s / $2f_0$
- 30log (OSR) = 96 – 6 + 5.17 = 95.17

A doubling of the OSR gives an SNR improvement of 9 dB / octave for a 1st order modulator;

95.17 / 9 = 10.57 $\qquad$ $2^{10.56}$ x 2*25 kHz = 75.48 MHz

OR: log(OSR)=95.17/30 = 3.17 → OSR = 1509.6

1509.6 * (2*25kHz) = 75.48 MHz

Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \quad (14.3$$

We see here that doubling the OSR improves the SNR for a second-order modulator by 15 dB or, equivalently, a gain of 2.5 bits/octave.

The realization of the second-order modulator using switched-capacitor techniques is straightforward and is left as an exercise for the interested reader.

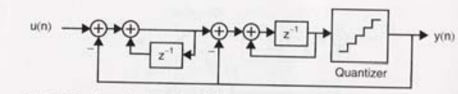


Fig. 14.10 Second-order ΔΣ modulator.

- Oversampling with 2nd order noise shaping:
- 6 – 12.9 + 50 log(OSR) = 96 $\qquad$ OSR = fs / $2f_0$
- 50 log (OSR) = 96 – 6 + 12.9 = 102.9

A doubling of the OSR gives an SNR improvement of 15 dB / octave for a 2nd order modulator;

102.9 / 15 = 6.86 $\qquad$ $2^{6.86}$ x 2*25 kHz = 5.81 MHz

2nd order sigma delta modulator

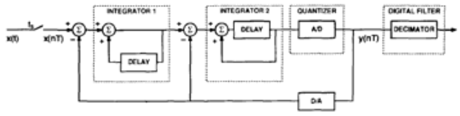


Fig. 1. Block diagram of second-order ΣΔ modulator with decimator.

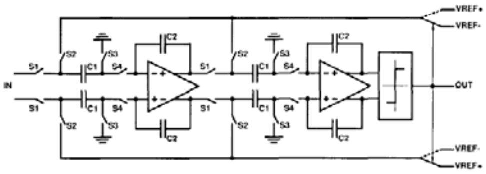


Fig. 10. Second-order ΣΔ modulator implementation.

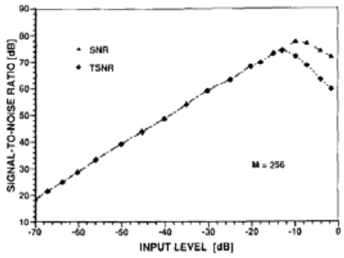


Fig. 13. Measured SNR for a sampling frequency of 4 MHz and a signal frequency of 1.02 kHz.

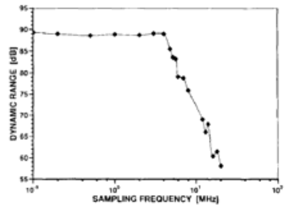
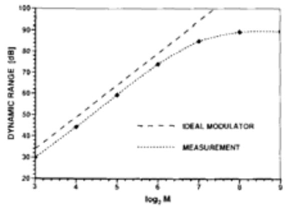


Fig. 14. Maximum operating frequency.



15. Dynamic range as a function of the oversampling ratio for a sampling frequency of 4 MHz.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 23, NO. 6, DECEMBER 1988

The Design of Sigma-Delta Modulation Analog-to-Digital Converters

BERNHARD E. BOSER, STUDENT MEMBER, IEEE, AND BRUCE A. WOOLEY, FELLOW, IEEE

14.3 System Architectures (A/D)

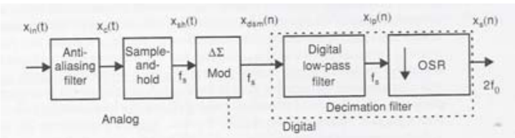
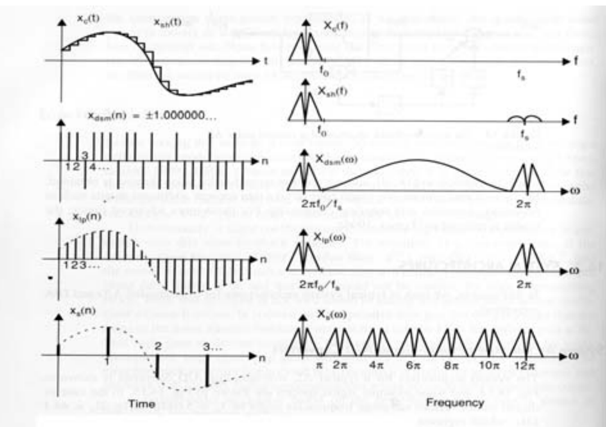


Fig. 14.14 Block diagram of an oversampling A/D converter.



- $X_c(t)$ is sampled and held, resulting in $x_{sh}(t)$.
- $x_{sh}(t)$ is applied to an A/D Sigma Delta modulator which has a 1-bit output, $x_{dsm}(n)$. The 1-bit signal is assumed to be linearly related to the input $X_c(t)$ (accurate to many orders of resolution), although it includes a large amount of out-of-band quantization noise (seen to the right).
- A digital LP filter removes any high frequency content, including out of band quantization noise, resulting in $X_{lp}(n)$
- Next, $X_{lp}(n)$ is resampled at $2f_0$ to obtain $X_s(n)$ by keeping samples at a submultiple of the OSR

System Architectures (D/A)

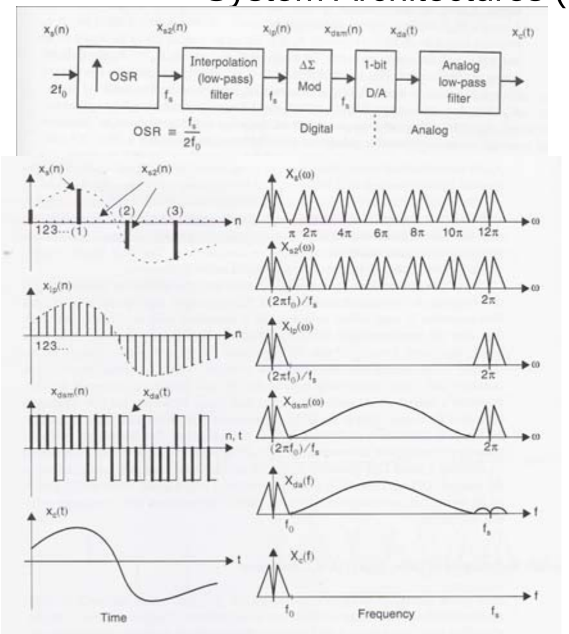


Fig. 14.17 Signals and spectra in an oversampling D/A converter.

- The digital input, $X_s(n)$ is a multi-bit signal and has an equivalent sample rate of $2f_0$, where f_0 ,is slightly higher than the highest input signal frequency.
- Since $X_s(n)$ is just a series of numbers the frequency spectrum has normalized the sample rate to 2π.
- The signal is upsampled to an equivalent higher sampling rate, f_s, resulting in the signal $x_{s2}(n)$
- $x_{s2}(n)$ has images left that are filtered out by the interpolation filter (brick-wall type) to create the multi-bit signal $X_{lp}(n)$, by digitally filtering out the images.
- $X_{lp}(n)$ is applied to a fully digital sigma delta modulator producing the 1-bit signal, $X_{dsm}(n)$, containing shaped quantization noise.
- $X_{dsm}(n)$ is fed to a 1-bit D/A producing $X_{da}(t)$, which has excellent linearity properties but still quantization noise.
- The desired signal, $X_c(t)$ can be obtained by using an analog filter to filter out the out-of-band quantization noise. (filter should be at least one order higher than the modulator.)

14.4 Digital decimation filters

- Many techniques
- a) FIR filter removes much of the quantization noise, so that the output can be downsampled by a 2nd stage filter which may be either IIR type (as in a), uppermost) or a cascade of FIR filters (as in b), below)
- In b) a few halfband FIR filters in combination with a sinc compensation FIR-filter are used.
In some applications, these halfband and sinc compensation filters can be realized using no general multi-bit multipliers [Saramaki, 1990]

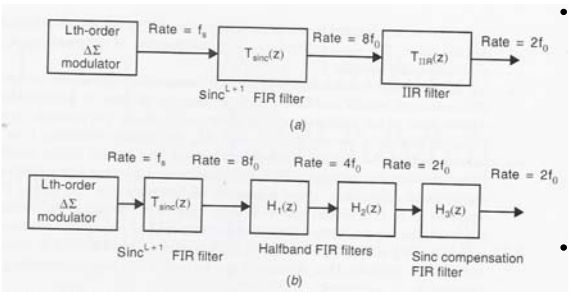


Fig. 14.18 Multi-stage decimation filters: (a) sinc followed by an IIR filter; (b) sinc followed by halfband filters.

14.5 Higher-Order Modulators – Interpolative structure

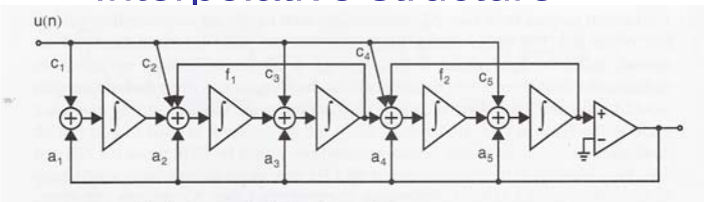


Fig. 14.20 A block diagram of a fifth-order modulator.

- Lth order noise shaping modulators improve SNR by 6L+3dB/octave.
- Typically a single high-order structure with feedback from the quantized signal.
- In figure 14.20 a single-bit D/A is used for feedback, providing excellent linearity.
- Unfortunately, modulators of order two or more can go unstable, especially when large input signals are present (and may not return to stability) Guaranteed stability for an interpolative modulator is nontrivial.

Multi-Stage Noise Shaping architecture ("MASH")

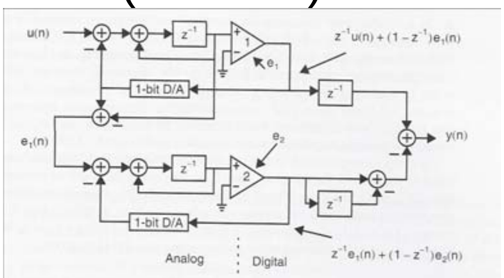
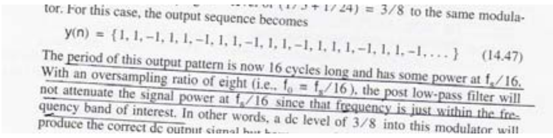


Fig. 14.21 A second-order MASH modulator using two first-order modulators. Note that the output, y(n), is a four-level signal.

- Overall higher order modulators are constructed using lower-order, more stable, ones → more stable overall system.
- Fig. 14.21: 2nd order using two first-order modulators.
- Higher order noise filtering can be achieved using lower-order modulators.
- Unfortunately sensitive to finite opamp gain and mismatch

14.7 Practical considerations

- Stability
- Linearity of two-level converters
- Idle tones
- Dithering
- Opamp gain



tor. For this case, the output sequence becomes

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, \dots\} \quad (14.47)$$

The period of this output pattern is now 16 cycles long and has some power at $f_s/16$. With an oversampling ratio of eight (i.e., $f_0 = f_s/16$), the post low-pass filter will not attenuate the signal power at $f_s/16$ since that frequency is just within the frequency band of interest. In other words, a dc level of 3/8 into this modulator will produce the correct dc output signal but ...

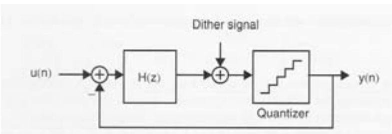
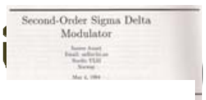


Fig. 14.26 Adding dithering to a delta-sigma modulator. Note that the dithered signal is also noise shaped.

Design example, 14b 2nd order Sigma-Delta mod



BOSER AND WOOLEY: SIGMA-DELTA MODULATION ANALOG-TO-DIGITAL CONVERTERS

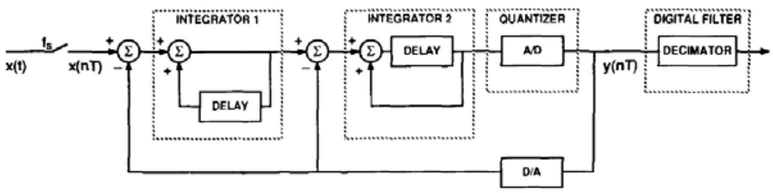


Fig. 1. Block diagram of second-order ΣΔ modulator with decimator.

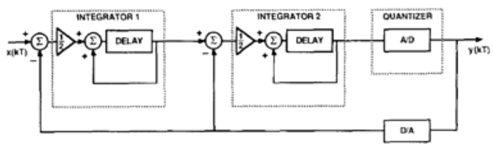


Fig. 2. Modified architecture of second-order ΣΔ modulator.

- 16 bit, 24 kHz , OSR as powers of two, and allowing for increased baseband noise due to nonidealities: OSR 512 was chosen

Design example, 14b 2nd order Sigma-Delta mod

- Among most relevant nonidealities:
- Finite DC gain
- Bandwidth,
- Slew rate
- Swing limitation
- Offset voltage
- Gain nonlinearity
- Flicker noise
- Sampling jitter
- Voltage dependent capacitors
- Switch on-resistance
- Offset voltage and settling time for comparators

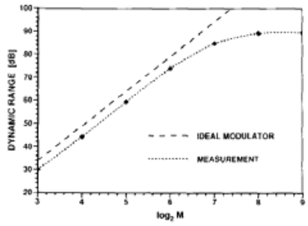
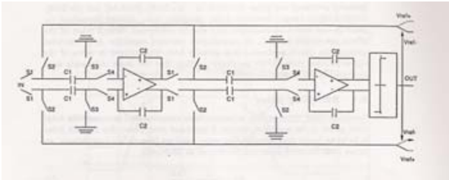
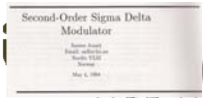
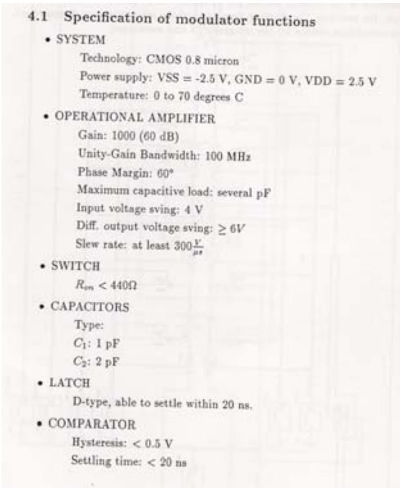


Fig. 15. Dynamic range as a function of the oversampling ratio for a sampling frequency of 4 MHz.



Design example, 14b 2nd order Sigma-Delta mod


Second-Order Sigma Delta Modulator



4.1 Specification of modulator functions

- SYSTEM
  - Technology: CMOS 0.8 micron
  - Power supply: VSS = -2.5 V, GND = 0 V, VDD = 2.5 V
  - Temperature: 0 to 70 degrees C
- OPERATIONAL AMPLIFIER
  - Gain: 1000 (60 dB)
  - Unity-Gain Bandwidth: 100 MHz
  - Phase Margin: 60°
  - Maximum capacitive load: several pF
  - Input voltage sving: 4 V
  - Diff. output voltage sving: $\geq 6V$
  - Slew rate: at least $300\frac{V}{\mu s}$
- SWITCH
  - $R_{on} < 440\Omega$
- CAPACITORS
  - Type:
  - C_1: 1 pF
  - C_2: 2 pF
- LATCH
  - D-type, able to settle within 20 ns.
- COMPARATOR
  - Hysteresis: < 0.5 V
  - Settling time: < 20 ns

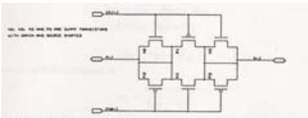


Figure 11: Dummy switch charge injection

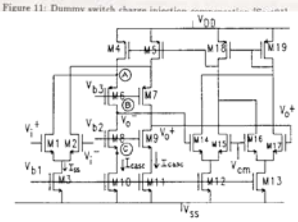
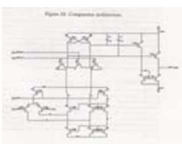
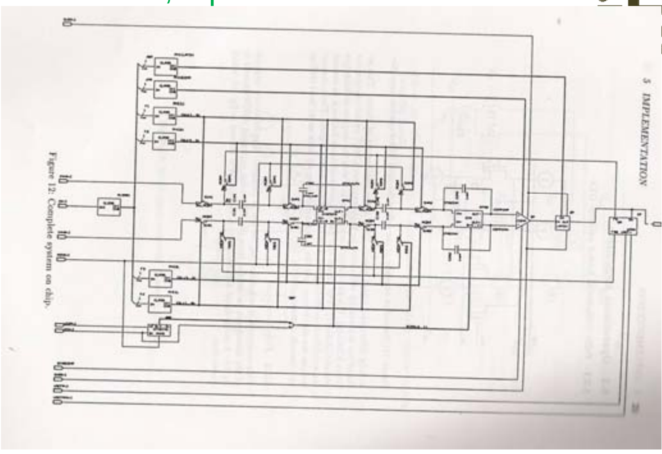


Fig. 1. Fully differential folded-cascode amplifier (after [4]).



- Noninverting parasitic insensitive integrator (fig 10.9) was used (fully differential implementation)

2nd order modulator; top level schematics



- Two-phase clock generator, switches, chopper stabilized OTA (1st int.), OTA (2nd int.- fully differential folded cascode), comparator, latch, two-level DAC. Biasing circuit. Functional after test.

Sigma Delta converters,ISSCC 2011

- ISSCC- Foremost global forum
- "CT": continous time

SESSION 27 **Wednesday February 23rd, 1:30 PM**

OVERSAMPLING CONVERTERS

Session Chair: **Kong-Pang Pun,** *Chinese University of Hong Kong, Hong Kong, China*
Associate Chair: **Lucien Breems,** *NXP, Eindhoven, The Netherlands*

27.1 A 4GHz CT ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW **1:30 PM**
M. Bolatkale[1], L. Breems[1], R. Rutten[1], K. Makinwa[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands

A 4GHz CT ΣΔ ADC is presented with a loop filter topology that absorbs the pole caused by the input capacitance of its 4b quantizer and compensates for the excess delay caused by the quantizer's latency. Implemented in 45nm CMOS, the ADC achieves 70dB DR and -74dBFS THD in a 125MHz BW, while dissipating 256mW and occupying only $0.9mm^2$.

27.2 An 8mW 50MS/s CT ΔΣ Modulator with 81dB SFDR and Digital Background DAC Linearization **2:00 PM**
J. G. Kauffman, P. Witte, J. Becker, M. Ortmanns
Ulm University, Ulm, Germany

A 3rd-order single-loop CT ΔΣ modulator with a 4b quantizer is sampled at 500MHz with an OSR of 10. It achieves 63.5dB SNDR and -81dB SFDR in a 25MHz bandwidth without DEM. The DAC nonlinearity is digitally estimated and corrected. All feedback amplifiers are compensated for finite GBW influence. The modulator occupies $0.15mm^2$ in 90nm CMOS and achieves an FOM of 125fJ/conversion-step.

27.3 A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bidirectional Single-Slope Quantizer **2:30 PM**
N. Maghari, U-K. Moon
Oregon State University, Corvallis, OR

A single-slope quantizer using modified bidirectional discharging is proposed. This quantizer provides first-order shaping of quantization noise and is used as the quantizer of a second-order delta-sigma loop. The fabricated prototype ADC achieves 78.2dB SNDR at 50MHz sampling speed at OSR of 24 with 2.9mW power consumption.

Break 3:00 PM

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SESSION 27 **Wednesday February 23rd, 1:30 PM**

27.4 A 250mV 7.5μW 61dB SNDR CMOS SC ΔΣ Modulator Using a Near-Threshold-Voltage-Biased CMOS Inverter Technique **3:15 PM**
F. Michel, M. Steyaert
KU Leuven, Leuven, Belgium

An ultra-low-voltage SC ΔΣ converter using a near-threshold-voltage-biasing technique is reported. This guarantees reliable operation of inverter-based integrators over temperature while running at a supply voltage of 250mV. An SNDR of 61dB is achieved for a BW of 10 kHz with a total power consumption of only 7.5μW.

27.5 A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-Amp Third-Order ΔΣ Modulator Consuming 140μW **3:45 PM**
A. Pena Perez, E. Bonizzoni, F. Maloberti
University of Pavia, Pavia, Italy

A third-order ΔΣ modulator with single operational amplifier achieves 13.6 bits with 100kHz signal bandwidth and consumes 140μW. The time-interleaved two-integrators scheme is a modification of a second-order prototype. A slew-rate boost enables minimum power in a two stages op-amp. The SFDR is 96dB with an FoM of 54fJ/conversion-step.

27.6 A 1.7mW 11b 1-1-1 MASH ΔΣ Time-to-Digital Converter **4:15 PM**
Y. Cao[1,2], P. Leroux[1,3], W. De Cock[2], M. Steyaert[1]
[1]KU Leuven, Leuven, Belgium
[2]SCK-CEN, Mol, Belgium
[3]KH Kempen, Geel, Belgium

The first radiation tolerant third-order ΔΣ TDC is presented. The converter, implemented in 0.13μm CMOS, employs a 1-1-1 MASH architecture. It achieves an ENOB of 11b and a time resolution of 5.6ps, when the OSR is 250. A radiation assessment up to 5MGy proves the TDC's robustness. The TDC core consumes 1.7mW and occupies $0.11mm^2$.

27.7 A 120dB-SNR 100dB-THD+N 21.5mW/Channel Multibit CT ΔΣ DAC **4:45 PM**
A. Bandyopadhyay, M. Determan, S. Kim, K. Nguyen
Analog Devices, Wilmington, MA

A continuous-time 8b oversampling DAC architecture is presented, which measures 120dB of SNR and 100dB of THD+N while consuming 21.5mW/channel. This performance is achieved by using a 3-level rotational data-shuffling scheme along with analog low-power techniques. The $1.35mm^2$/channel chip is fabricated in 0.35μm DPQM CMOS process.

27.8 A 108dB-DR 120dB-THD and $0.5V_{rms}$ Output Audio DAC with Inter-Symbol-Interference-Shaping Algorithm in 45nm CMOS **5:15 PM**
L. Risbo[1], R. Hezar[2], B. Kelleci[2], H. Kiper[2], M. Fares[2]
[1]Texas Instruments, Copenhagen, Denmark
[2]Texas Instruments, Dallas, TX

An oversampled audio multi-bit DAC using a mismatch-shaping algorithm designed to shape element mismatch errors concurrently with inter-symbol-interference is presented. It can achieve THD powers better than -120dBFs with spurious tone free operation at low signal levels. It is implemented in 45nm CMOS with $0.16mm^2$ area, 0.875mW power, and $0.5V_{rms}$ output.

Conclusion 5:45 PM

litterature

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A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35-µM CMOS FOR LOW FREQUENCY APPLICATIONS

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Next week, 22/3-11

- Ch. 13; Nonlinearity and Mismatch plus beginning of chapter 14; Oscillators (?)
- Messages are given on the INF4420 homepage.

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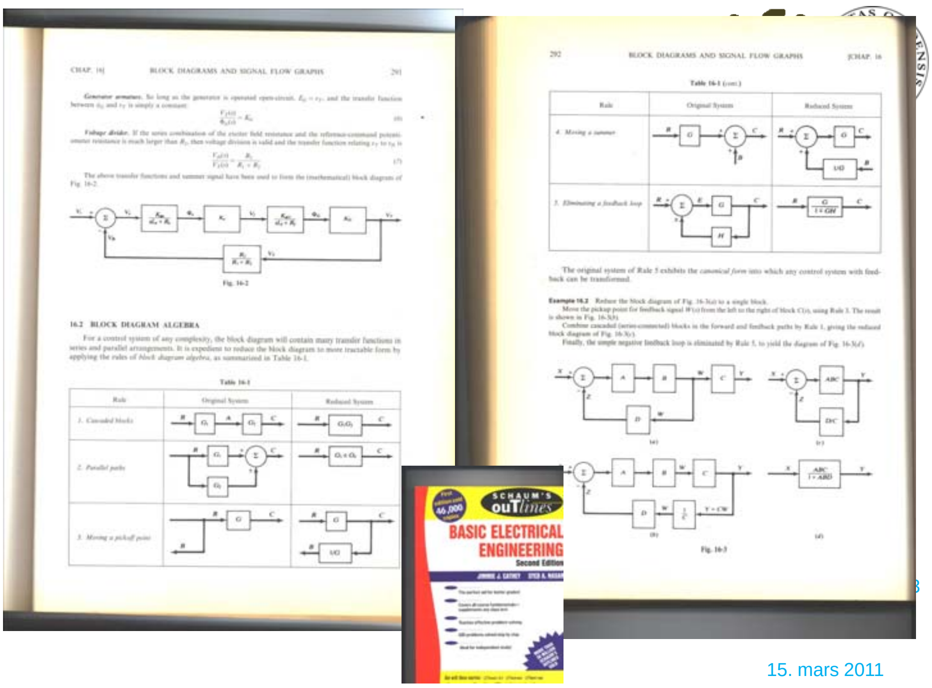
CHAP. 16]
BLOCK DIAGRAMS AND SIGNAL FLOW GRAPHS
Fig. 16-2
16.2 BLOCK DIAGRAM ALGEBRA
For a control system of any complexity, the block diagram will contain many transfer functions in series and parallel arrangements. It is expedient to reduce the block diagram to more tractable form by applying the rules of block diagram algebra, as summarized in Table 16-1.
Table 16-1
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BLOCK DIAGRAMS AND SIGNAL FLOW GRAPHS
[CHAP. 16
Fig. 16-3
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