Nonlinearity and mismatch

Tuesday, March 22nd, 9:15 – 11:00

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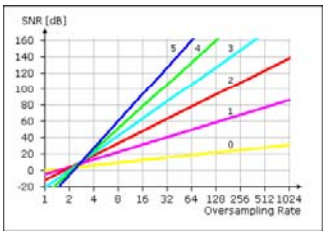
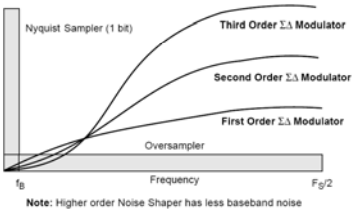
Last time – and today, Tuesday 22nd of March:

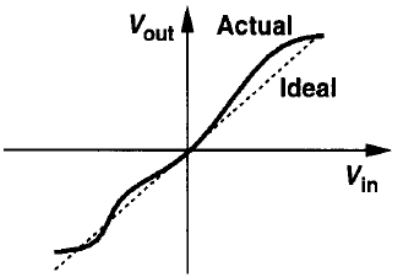
Last time:

From chapters 13 and 14 in Razavi;
Nonlinearity and Mismatch and
Oscillators:
13.1 Nonlinearity
13.1.1 general considerations
13.1.2 nonlinearity and differential circuits
13.1.3 effects of negative feedback on nonlin.
13.1.4 capacitor nonlinearity
13.1.5 linearization techniques
13.2 Mismatch
DC offsets, even order distortion,
13.2.1 offset cancellation techniques
13.2.2 reduction of noise by offset cancellation
Last time, from chapter 14 in "J. & M.":
14.1 Oversampling without noise shaping
14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
2nd order sigma delta design example



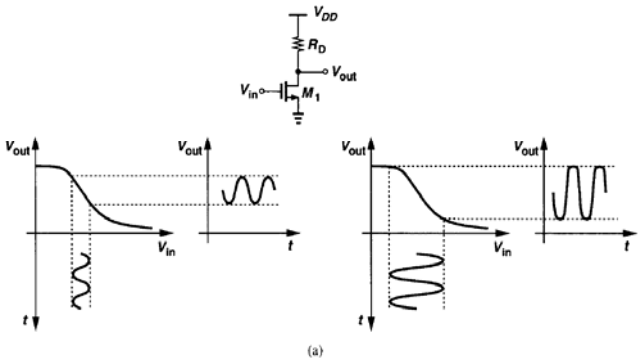


I/O characteristic of a nonlinear system



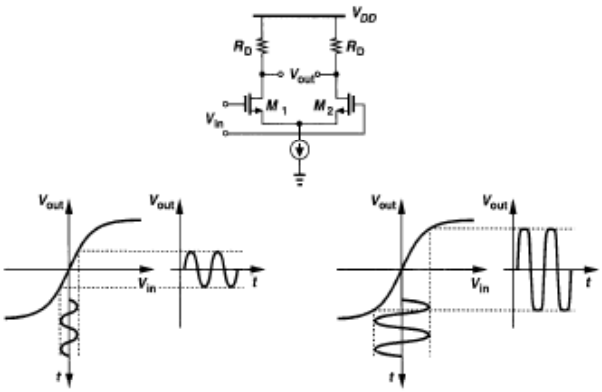
- Imperfection that is critical in high precision analog circuits
- Characteristic deviates from a straight line as the input swing increases

Distortion in common-source stage



- The output is a reasonable replica of the input for small input swing, but for large output swings the output exhibits ”saturated” levels.

Distortion in a differential pair



- The output is a reasonable replica of the input for small input swing, but for large output swings the output exhibits ”saturated” levels.

Variation in small signal gain and definition of nonlinearity

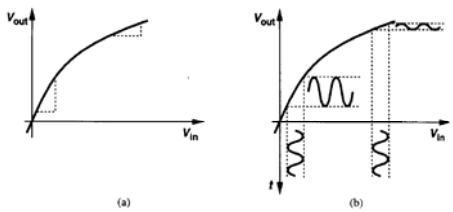


Figure 13.3 Variation of small-signal gain in a nonlinear amplifier.

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots.$$

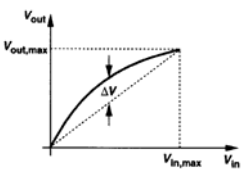


Figure 13.4 Definition of nonlinearity.

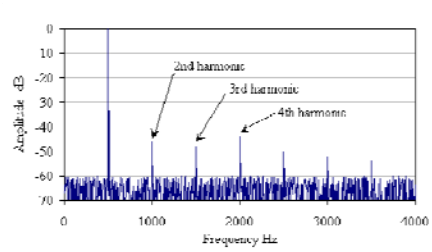
- Fig. 13.3: A given incremental change at the input results in different incremental changes at the output depending on input dc level.
- May approximate I/O characteristics by a Taylor expansion in the range of interest.
- For small x, $y(t) \approx \acute{\alpha}_1 x$, where $\acute{\alpha}_1$ is the small signal gain in the vicinity of $x \approx 0$.
- A method to quantify nonlinearity is to identify the coefficients in eq. 13.1
- Another useful metric is to specify the maximum deviation from an ideal characteristic (See Fig. 13.4)

Total Harmonic Distortion ("THD")

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3\cos^3\omega t + \cdots \quad (13.8)$$

$$= \alpha_1 A\cos\omega t + \frac{\alpha_2 A^2}{2}[1+\cos(2\omega t)] + \frac{\alpha_3 A^3}{4}[3\cos\omega t + \cos(3\omega t)] + \cdots. \quad (13.9)$$

$$THD = \frac{(\alpha_2 A^2/2)^2 + (\alpha_3 A^3/4)^2}{(\alpha_1 A + 3\alpha_3 A^3/4)^2}. \quad (13.10)$$



$$\text{THD} = \frac{P_2 + P_3 + P_4 + \cdots + P_\infty}{P_1} = \frac{\sum_{n=2}^{\infty} P_n}{P_1}$$

- The nonlinearity can be characterized by applying a sinusoid at the input and measuring the harmonic content of the output.
- Even-order terms and odd-order terms result in even and odd harmonics.
- The magnitude of the nth harmonic grows roughly in portion to the nth power of the input amplitude.
- The harmonic distortion is usually quantified by summing the power of all of the harmonics (except that of the fundamental) and normalizing the result to the power of the fundamental.
- Eq. 13.10 is for a 3rd order nonlinearity.
- CD: THD of about 0.01 % (-80 dB), Video: THD of about 0.1 % (-60 dB).

Nonlinearity of differential circuits

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) + \cdots,$$

$$|A_v| \approx g_m R_D$$

$$= \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})R_D.$$

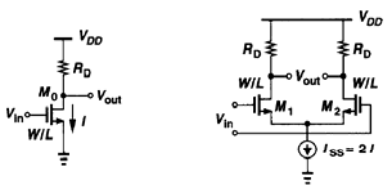


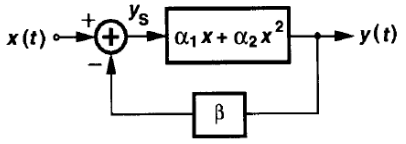
Figure 13.6 Single-ended and differential amplifiers providing the same voltage gain.

$$\frac{A_{HD2}}{A_F} = \frac{V_m}{4(V_{GS} - V_{TH})}. \quad (13.15)$$

$$\frac{A_{HD3}}{A_F} \approx \frac{V_m^2}{32(V_{GS} - V_{TH})^2}. \quad (13.22)$$

- Odd-symmetric I/O characteristics
- Small signal voltage gain for both amplifiers in Fig. 13.6 given by $|Av|$
- Equations 13.15 (amplitude of the 2nd harmonic) and 13.22 indicate that the differential circuit exhibits much less distortion than its single ended counterpart while providing the same voltage gain and output swing.
- For example if Vm = 0.2(V_{GS}-V_{TH}), (13.15 and 13.22) yield a distortion of 5 % and 0.125 %, respectively.
- Diff. Solution consumes twice as much power.

Effect of Negative feedback on Nonlinearity



$y \approx a \cos \omega t + b \cos 2\omega t.$[1]

For a meaningful comparison, we normalize the amplitude of the second harmonic to that of the fundamental:

$$\frac{b}{a} = \frac{\alpha_2 V_m}{2} \frac{1}{\alpha_1} \frac{1}{(1+\beta\alpha_1)^2}. \tag{13.36}$$

Without feedback, on the other hand, such a ratio would be equal to $(\alpha_2 V_m^2/2)/\alpha_1 V_m = \alpha_2 V_m/(2\alpha_1)$. Thus, the relative magnitude of the second harmonic has dropped by a factor of $(1+\beta\alpha_1)^2$.

- Sinusoidal input x(t) = Vm cosωt
- Employing feedback reduces the relative magnitude of the 2nd harmonic by of $(1+\beta\alpha_1)^2$

Capacitor nonlinearity due to voltage dependence (for noninverting amplifier from Fig. 12.41)

To study the effect of capacitor nonlinearity, we express each capacitor as $C = C_0(1 + \alpha_1 V + \alpha_2 V^2 + \cdots)$.

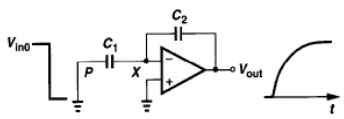


Figure 13.9 Effect of capacitor nonlinearity.

$$Q_1 = \int_0^{V_{in0}} C_1\, dV \tag{13.38}$$

$$= \int_0^{V_{in0}} MC_0(1+\alpha_1 V)\, dV \tag{13.39}$$

$$= MC_0 V_{in0} + MC_0 \frac{\alpha_1}{2} V^2. \tag{13.40}$$

$$Q_2 = \int_0^{V_{out}} C_2\, dV \tag{13.41}$$

$$= C_0 V_{out} + C_0 \frac{\alpha_1}{2} V_{out}^2. \tag{13.42}$$

Equating Q_1 and Q_2 and solving for V_{out}, we have

$$V_{out} = \frac{1}{\alpha_1}\left(-1 + \sqrt{1 + M\alpha_1^2 V_{in0}^2 + 2M\alpha_1 V_{in0}}\right). \tag{13.43}$$

The last two terms under the square root are usually much less than unity and, since for $\epsilon \ll 1$, $\sqrt{1+\epsilon} \approx 1 + \epsilon/2 - \epsilon^2/8$, we can write

$$V_{out} \approx MV_{in0} + (1-M)\frac{M\alpha_1}{2} V_{in0}^2. \tag{13.44}$$

The second term in the above equation represents the nonlinearity resulting from the voltage dependence of the capacitor.

- In SC circuits voltage dependence of capacitors may introduce substantial distortion.

Linearization – reducing the dependence of the gain of the circuit upon the input level.

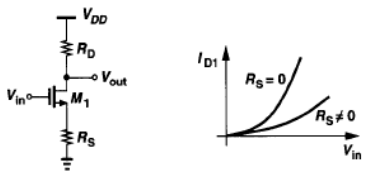


Figure 13.10 Common-source stage with resistive degeneration.

$$G_m = \frac{g_m}{1 + g_m R_S}, \qquad (13.45)$$

- Source degeneration by means of a linear resistor of the transistor, making the I/O characreduces the swing applied between the gate and the source teristics more linear.

  The overall transconductance of the stage may be written as in eq. 13.45., which for large $g_m R_s$ approaches $1/R_s$, an input-independent value.
- The amount of linearization depends on $g_m R_s$ rather on R_s alone.
- Resistive degenartion presents tradeoffs between linearity, noise, power dissipation and gain. For reasonable voltage swings (e.g. 1 Vpp) it may be quite difficult to achieve even a voltage gain of 2 in a common-source stage if the nonlinearity is to remain below 1 %.

Degeneration of differential pair

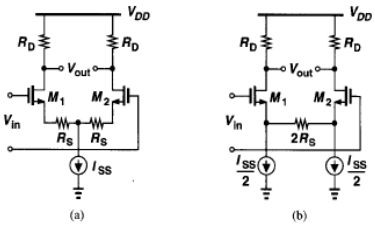


Figure 13.11 Source degeneration applied to a differential pair.

- A differential pair can be degenerated as shown in Figs. 13.11 a) and b)
- In Fig. 13.11 a) I_{SS} flows through the degenartion resistors, consuming a voltage headroom of $I_{SS}R_S/2$, which can become an issue if a high level of degeneration is required.
- The circuit in Fig. 13.11 b) suffers from a slightly higher noise and offset voltage because the two tail current sources introduce some differential error.

Degeneration of differential pair

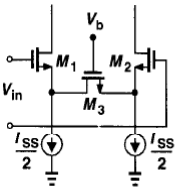


Figure 13.12 Differential pair degenerated by a MOSFET operating in deep triode region.

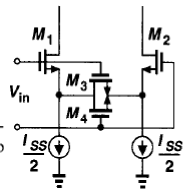


Figure 13.13 Differential pair degenerated by two MOSFETs operating in the triode region.

- High-quality resistors for resistive degeneration are not available in many of today's CMOS technologies.
- As depicted in Fig. 13.12 it can be replaced by a MOSFET operating in deep triode region.
- For large inputs M_3 may not remain in deep triode region, thereby experiencing substantial change in its on-resistance.
- V_b must track the input common mode level so that R_{on3} can be defined accurately.
- Fig. 13.13 shows a solution where the circuit remains relatively linear even if one degeneration device goes into saturation.

Linearization of differential pair avoiding the use of resistors

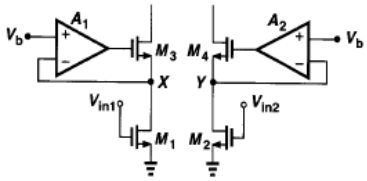


Figure 13.14 Differential pair using input devices operating in the triode region.

- Based on the observation that a MOSFET operating in the triode region can provide a linear I_D/V_{GS} characteristic if its drain-source voltage is held constant.
- Forces Vx and Vy to be equal to Vb for varying input levels.
- Drawbacks: transconductance of M1 and M2 relative small. Input common-mode level must be tightly controlled. M3, M4 and the two amplifiers contribute substantial noise to the output.

Linearization technique viewing the amplifier as a V/I converter followed by a I/V converter.

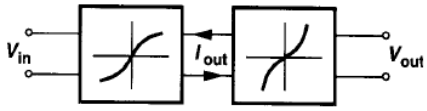


Figure 13.15 Voltage amplifier viewed as a cascade of two nonlinear stages.

- If V/I converter: V/I : $I_{out} = f(V_{in})$, I/V converter: $V_{out} = f^{-1}(I_{in})$, then the output voltage is a linear function of the input voltage.

Mismatch

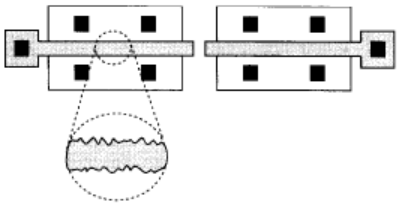
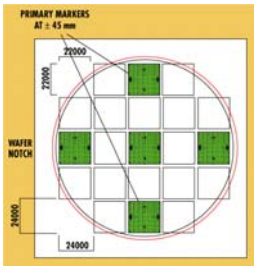


Figure 13.17 Random mismatches due to microscopic variations in device dimensions.



- MOSFETs suffer from random, microscopic variations and hence mismatches between the equivalent lengths and widths of two transistors that are identically laid out.
- Study of mismatch:
- 1) mechanisms behind
- 2) effect of mismatches
- Layout techniques in chapter 18.

Mismatch – wide MOSFET from parallell devices reducing the variation in L.

Expressing the characteristics of a MOSFET in saturation as $I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$, we observe that mismatches between μ, C_{ox}, W, L, and V_{TH} result in mismatches between drain currents (for a given V_{GS}) or gate-source voltages (for a given drain current) of two nominally-identical transistors. Intuitively, we expect that as W and L in-

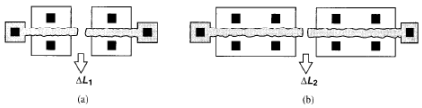


Figure 13.18 Reduction of length mismatch as a result of increasing the width.

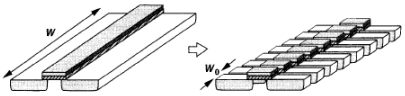


Figure 13.19 Wide MOSFET viewed as a parallel combination of narrow devices.

$$\Delta L_{eq} \approx \left(\Delta L_1^2 + \Delta L_2^2 + \cdots + \Delta L_n^2\right)^{1/2}/n \quad (13.57)$$

$$= \frac{\left(n\Delta L_0^2\right)^{1/2}}{n} \quad (13.58)$$

$$= \frac{\Delta L_0}{\sqrt{n}}, \quad (13.59)$$

- All of the mismatches decrease as the area of the transistor, WL, increases.
- As WL increases, random variations experience greater "averaging", thereby falling in magnitude.
- Fig. 13.18; $\Delta L_2 < \Delta L_1$ because the device is viewed as many small transistors.
- Fig. 13.19: Each transistor having a width W0, with an equivalent length as $L_{eq} \approx (L_1 + L_2 + \cdots + L_n)/n.$
- Overall variation given by 13.59. n increases → variation in length decreases

Mismatch reduction ; decomposing in series and parallell combination of small unit transistors

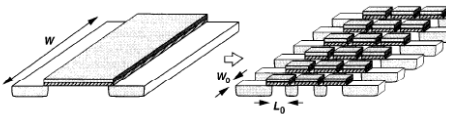
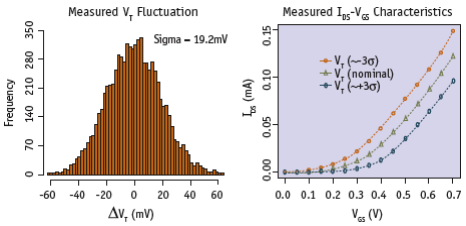


Figure 13.20 Large MOSFET viewed as a combination of small devices.

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \quad (13.60)$$

$$\Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}. \quad (13.61)$$

- Relations in Eq. 13.60 and 13.61 show that mismatch is reduced when WL increases (have been verified mathematically and experimentally).
- **Characterizing process variation in nanometer CMOS**
- By **Kanak Agarwal** , EDA Tech forum



Mismatch and dc offset

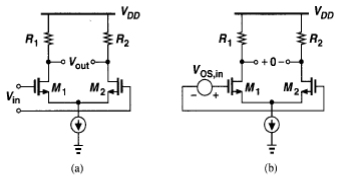


Figure 13.21 (a) Differential pair with offset measured at the output, (b) circuit of (a) with its offset referred to the input.

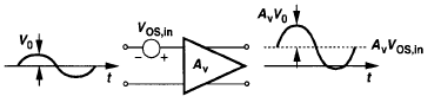


Figure 13.22 Effect of offset in an amplifier.

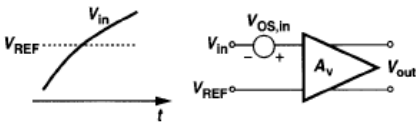
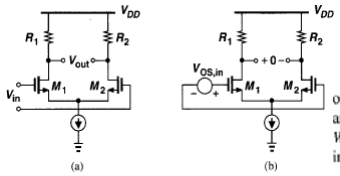


Figure 13.23 Accuracy limitation of an amplifier due to offset.

- Device mismatch leads to dc offsets, finite even-order distortion and lower common-mode rejection, which reduce performance of circuits.
- In Fig. 13.22 the output contains amplified replicas of both the signal and the offset. In a cascade of direct-coupled amplifiers the dc offset may experience so much gain that it drives the latter stages into nonlinear operation.
- If an amplifier is used to determine whether the input signal is greater than or less tha a reference, V_{REF}, then the input-referred offset imposes a lower bound on the minimum V_{in} -V_{REF} that can be detected reliably

Differential pair and calculation of offset voltage



our objective is to find the value of $V_{OS,in}$ such that $V_{out} = 0$. The device mismatches are incorporated as $V_{TH1} = V_{TH}$, $V_{TH2} = V_{TH} + \Delta V_{TH}$; $(W/L)_1 = W/L$, $(W/L)_2 = W/L + \Delta(W/L)$; $R_1 = R_D$, $R_2 = R_D + \Delta R$. For simplicity, $\lambda = \gamma = 0$, and mismatches in $\mu_n C_{ox}$ are neglected. For $V_{out} = 0$, we must have $I_{D1}R_1 = I_{D2}R_2$, concluding that I_{D1}

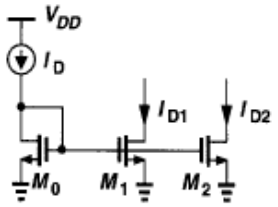
Figure 13.21 (a) Differential pair with offset measured at the output, (b) circuit of (a) with its offset referred to the input.

$$V_{OS,in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH}, \qquad (13.69)$$

$$V_{OS,in}^2 = \left(\frac{V_{GS} - V_{TH}}{2}\right)^2 \left\{\left(\frac{\Delta R_D}{R_D}\right)^2 + \left[\frac{\Delta(W/L)}{(W/L)}\right]^2\right\} + \Delta V_{TH}^2, \qquad (13.70)$$

- It is assumed that the input transistors and the load resistors suffer from mismatch.
- Want to find the input referred offset so that Vout = 0.
- Eq. 13.69 reveals dependence on device mismatches and biasing. The contribution of load resistor mismatch and transistor dimension mismatch increases with the equilibrium overdrive, and the threshold voltage mismatch is directly referred to the input.
- Eq. 13.69 may be expressed as in eq. 13.70, since mismatches are independent statistical variables.

Mismatch between current sources



$$\Delta y = \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \cdots. \quad (13.74)$$

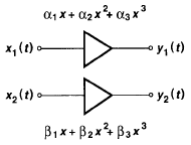
$$\Delta I_D = \frac{\partial I_D}{\partial (W/L)}\Delta\left(\frac{W}{L}\right) + \frac{\partial I_D}{\partial (V_{GS} - V_{TH})}\Delta(V_{GS} - V_{TH}), \quad (13.75)$$

$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}(V_{GS} - V_{TH})^2 \Delta\left(\frac{W}{L}\right) - \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\Delta V_{TH}. \quad (13.76)$$

$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{W/L} - 2\frac{\Delta V_{TH}}{V_{GS} - V_{TH}}. \quad (13.77)$$

- Eq. 13.77 suggests that to minimize current mismatch, the overdrive voltage must be maximized (, a trend opposite to Eq. 13.69, for the input referred offset voltage for a differential pair).
- As V_{GS} - V_{TH} increases, threshold voltage mismatch has lesser effect on the device currents.

Even order distortion

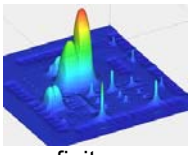


insight. Suppose the two signal paths in a differential circuit are represented by $y_1 \approx \alpha_1 x_1 + \alpha_2 x_1^2 + \alpha_3 x_1^3$ and $y_2 \approx \beta_1 x_2 + \beta_2 x_2^2 + \beta_3 x_2^3$ (Fig. 13.26). The differential output is given by

$$y_1 - y_2 = (\alpha_1 x_1 - \beta_2 x_2) + (\alpha_2 x_1^2 - \beta_2 x_2^2) + (\alpha_3 x_1^3 - \beta_3 x_2^3), \quad (13.78)$$

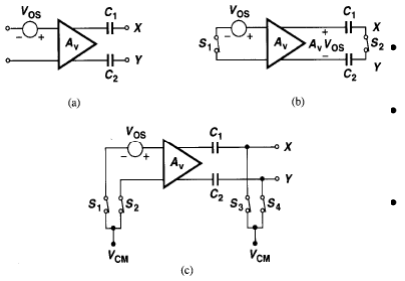
which, for $x_1 = -x_2$, reduces to

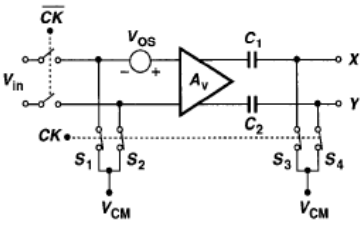
$$y_1 - y_2 = (\alpha_1 + \beta_1)x_1 + (\alpha_2 - \beta_2)x_1^2 + (\alpha_3 + \beta_3)x_1^3. \quad (13.79)$$



- Differential circuits should be free from even order distortion.
- In reality, mismatches degrade the symmetry, thereby introducing a finite even-order nonlinearity.
- Generally quite complex analysis.
- Two signal paths, Y_1 and Y_2, given in the Figure. The differential output is given by (13.78) and when $X_1 = -X_2$, by (13.79)
- If $x_1(t) = A \cos\omega t$, the 2nd order harmonic has an amplitude equal to $(\alpha_2 - \beta_2)A^2/2$, i.e. proportional to the mismatch between the 2nd order coefficients of the input/output characteristic.
- At high frequencies signals experience considerable phase shift. Therefore even-order distortion may arise from *phase* mismatch.
- Thermal gradients across chip may create asymmetries (Threshold voltages and mobilities)

Electronic Mismatch cancellation – ”output offset storage”





- Fig 13.27 b); driving $V_{out} = A_v V_{os}$, while nodes X and Y are shorted.
- When the node voltages have settled, a zero differential input results in a zero difference between Vx and Vy.
- Thus, after S1 and S2 turn off, the circuit consisting of the amplifier and C1 and C2 exhibits a zero offset voltage, amplifying only the *changes* in the differential input voltage.
- In practice the inputs and outputs must be shorted to proper common-mode voltages [Fig. 13.27 c)]
- This type of offset cancellation ”measures” the offset by setting the differential input to zero and stores the result on capacitors in series with the output.
- Fig. 13.28: CK denotes the offset cancellation command.

”input offset storage” offset cancellation technique

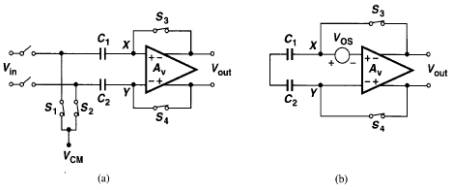


Figure 13.29 (a) Input offset storage, (b) circuit of (a) in the offset cancellation mode.

$$V_{out} = \frac{A_v}{1 + A_v} V_{OS} \quad (13.80)$$

$$\approx V_{OS}. \quad (13.81)$$

- For applications where higher gain (>10) is needed.
- Incorporates two series capacitors at the input and places the amplifier in a unity-gain negative feedback loop during offset cancellation.
- From Fig. 13.29 b) we get eq. 13.89 and 13.81.
- The offset is stored on C1 and C2. For zero differential input, the differential output is equal to V_{OS}.
- Drawbacks: Capacitors are introduced in the feedback path, which is a serious issue for opamp’s and feedback paths. The bottom plate parasitics may reduce the magnitude of the poles, degrading the phase margin. Settling speed may be limited.

Removing capacitors in the signal path, to avoid degradation of phase margin and settling speed

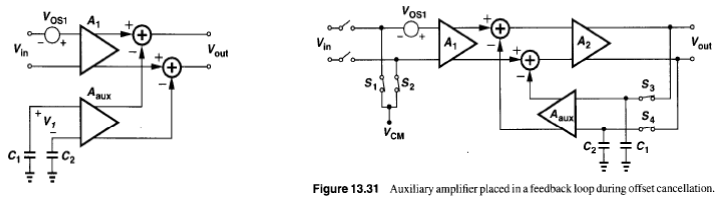


Figure 13.31 Auxiliary amplifier placed in a feedback loop during offset cancellation.

- Using an auxiliary amplifier,
- A_{aux} amplifies the differential voltage V_1 stored accross C_1 and C_2 and subtracts the result from the output of A_1.
- If $V_{OS1}A1 = V_1A_{aux}$, then for $V_{in} = 0$, $V_{out} = 0$, and the signal path is free of offsets.
- C_1 and C_2 not in the signal path.
- V_1 is generated like in Fig. 13.31, with the help of a 2nd stage, A_2.
- Operation; 1st: Only S_1 and S_2 on, yielding $V_{out} = V_{OS1}A_1A_2$. Now, assume S_3 and S_4 turn on, placing A_2 and A_{aux} in a negative feedback loop. Then V_{out} drops by a factor approximately equal to the loop gain: $V_{OS1}A_1A_2/(A_2A_{aux}) = V_{OS1}A_1/A_{aux.}$ Stored accross C_1 and C_2, this value is the required V1 in Fig. 13.30.
- Drawbacks: Two voltage gain stages in the signal path may not be desirable in a high-speed opamp. Addition of the voltages A1 and A2 is also difficult → Fig. 13.32.

”input offset storage” offset cancellation technique

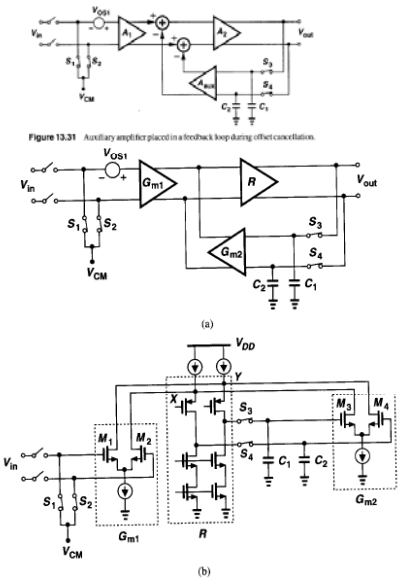


Figure 13.32 (a) Circuit of Fig. 13.31 using G_m and R stages, (b) realization of (a) in a folded-cascode op amp.

- Fig. 13.32 shows a similar solution avoiding the need of adding voltages A_1 and A_2.
- Each G_m stage is a differential pair and the R stage represents a transimpedance amplifier (or G_{m1} and R may constitute a one-stage opamp while G_{m2} adds an offset correction current).
- This technique is a usual realization.
- The techniques mentioned need periodic refreshing (a few kHz) because the junction and subthreshold leakage of the switches corrupt the correction voltage stored accross the capacitors.

Offset cancellation from Fig. 13.32 (upper)

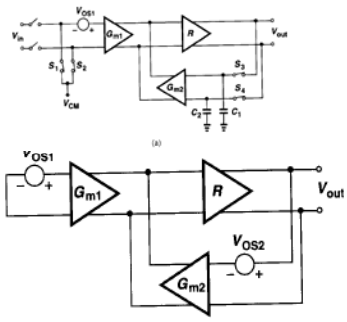


Figure 13.33 Circuit of Fig. 13.32(a) including offset of G_{m2}.

$$[G_{m1}V_{OS1} - G_{m2}(V_{out} - V_{OS2})]R = V_{out}. \quad (13.82)$$

$$V_{out} = \frac{G_{m1}RV_{OS1} + G_{m2}RV_{OS2}}{1 + G_{m2}R}. \quad (13.83)$$

$$V_{OS,tot} = \frac{V_{out}}{G_{m1}R} \quad (13.84)$$

$$= \frac{V_{OS1}}{1 + G_{m2}R} + \frac{G_{m2}}{G_{m1}}\frac{V_{OS2}}{1 + G_{m2}R} \quad (13.85)$$

$$\approx \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R}, \quad (13.86)$$

where we have assumed $G_{m2}R \gg 1$. If $G_{m2}R$ and $G_{m1}R$ are large, as in the op amp of Fig. 13.32(b), then $V_{OS,tot}$ is very small.

- Good cancellation of offset if $G_{m2}R$ and G_{m1} are large.
- Caution: Upon turning off, S_3 and S_4 may inject slightly unequal charges onto the two capacitors, creating an error voltage that is not corrected because the feedback loop is opened.
- Periodic refreshing needed

Reduction of noise by offset cancellation

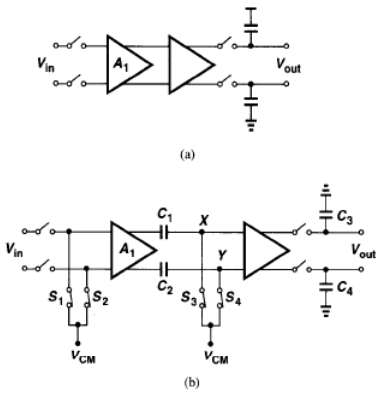
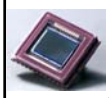
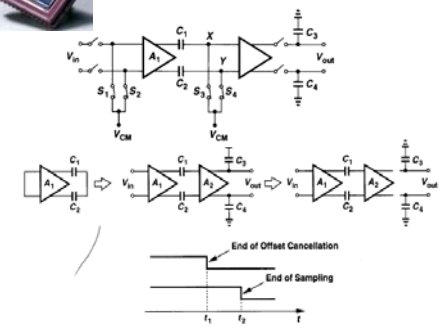


Figure 13.34 (a) Front end of a sampler, (b) circuit of (a) with offset cancellation applied to the first stage.

- Offset may be seen as a noise component having a very low frequency.
- It's therefore expected that periodic offset cancellation can potentially reduce low-frequency noise of the circuit as well.
- Fig. 13.34 a) Noise of A_1 directly corrupts V_{in}.
- 1/f noise of A_1 problematic if the signal spectrum extends from zero to only a few MHz, since the 1/f noise corner frequency is typically around 500 kHz to 1 MHz.
- Fig. 13.34 b) shows how the amplifier can undergo offset cancellation before every sampling operation.



Reduction of noise by offset cancellation



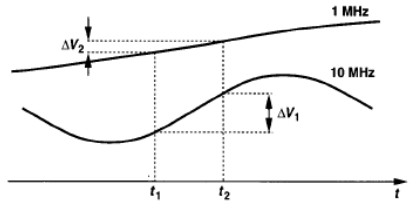


Figure 13.36 Variation of 1-MHz and 10-MHz noise components in a time interval of 10 ns.

- Offset cancellation before every sampling operation.
- From t_1 to t_2 (Fig. 13.36) , only high frequency components of A_1, in the order of $1/(t_2-t_1)$, change V_{XY} significantly. In other words the offset cancellation suppresses noise frequencies below roughly $1/(t_2-t_1)$.
- Noise frequencies that are below a certain frequency (here. A few MHz) do not have sufficient time to change if the sampling occurs only 10 ns after the end of offset cancellation.
- Called ”correlated double sampling”, originally used in charge coupled devices. Wide usage in suppressing 1/f noise. Leads to aliasing of wideband noise.

Preliminary plan for next week..

- http://www.uio.no/studier/emner/matnat/ifi/INF4420/v11/undervisningsplan.xml
- Oscillators (chapter 14 in ”Razavi”)