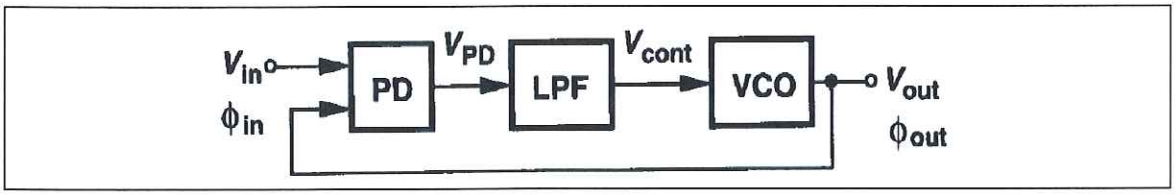
UNIVERSITY OF OSLO

Faculty of Mathematics and Natural Sciences

Exam in: INF9425 Projects in Analog / Mixed Signal CMOS Construction.
Day of exam: Tuesday, June the 6th, 2011.
Exam hours: 14:30 – 18:30.
This examination paper consists of 5 page(s).
Appendices: None.
Permitted materials: Any written material and approved calculator.

Make sure that your copy of this examination paper is complete before answering.

1 a) (Weight 6 %. Problems 1 a), b), c) and d) count as 22 % of the exam.)



A simplified schematic for a Phase-Locked-Loop is shown in the figure above, taken from "Design of Analog Integrated Circuits", by B. Razavi. Why isn't it a good idea to replace the low-pass filter ("LPF") for a high-pass filter? Please explain.

1 b) (Weight 8 %)

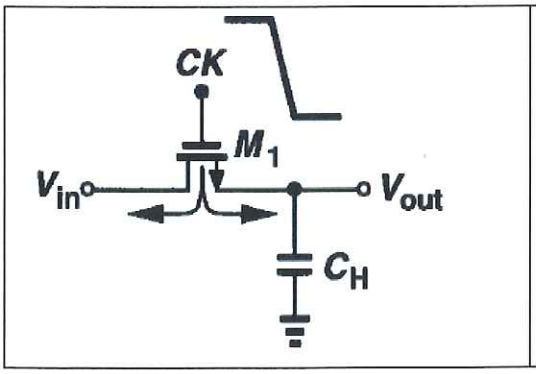


Table 2.1 Level 1 SPICE Models for NMOS and PMOS Devices.

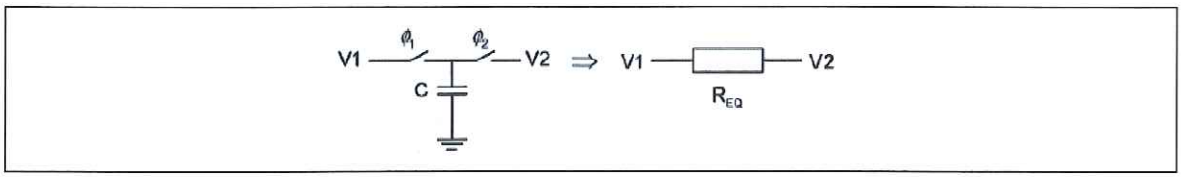
NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

In the schematics to the left, in the Figure above, $(W/L)_1$ = 15μm / 0.5 μm and the supply voltage 3 V. C_H = 10 pF. Use $C_{OX} = 3.83 \cdot 10^{-3}$ F/m^2 . Relevant device data are included in Table 2.1, to the right of the schematics. What is the error on V_{out}, due to charge injection? What would the worst case error due to clock feedthrough be?

1 c) (Weight 4 %)

Suppose that the supply voltage of a switched-capacitor amplifier is reduced by a factor of two and so is the maximum allowable output voltage swing. In order to maintain the dynamic range constant, the noise voltage must scale down by the same factor. If the noise is only of the kT/C type, how should the capacitors in the circuit be scaled?

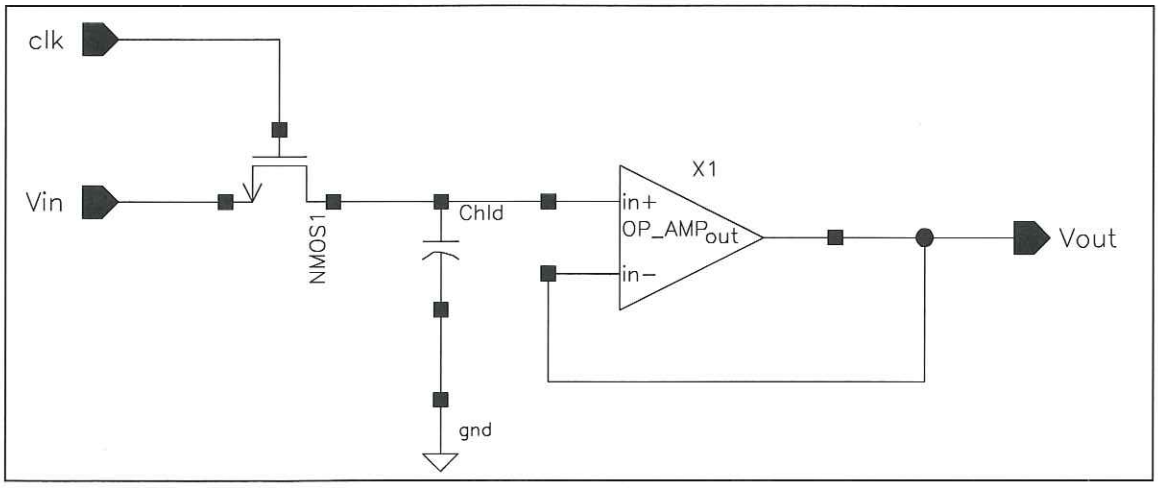
1 d) (Weight 4 %)



A switched-capacitor realization of a resistor, shown above, has an equal resistance, R_{EQ} of 1 MΩ, and is sampled at a clock frequency of 100 kHz. What is the size of the capacitance, C?

2 a) (Weight 4 %. Problems 2 a), b) and c) total 20 % of the exam.)

A simple sample-and-hold ("S/H") circuit is shown in the schematics below. It is implemented in a standard 90 nm CMOS technology, having a supply voltage of 1.0 V. The clock signal ("clk") varies between 0 V and 1 V, while a sine wave varying between 0.3 V AND 0.5 V is connected to the input ("Vin").



Consider the S/H from the Figure above, and assume $\mu_n C_{ox}$ = 134 μA / V^2, $(W/L)_{NMOS1}$ = 8μm/1μm V_{TH} = 0.35 V and γ = 0. Assume that the input of the voltage follower tracks Vin with negligible phase shift. Calculate the maximum on-resistance of the switch.

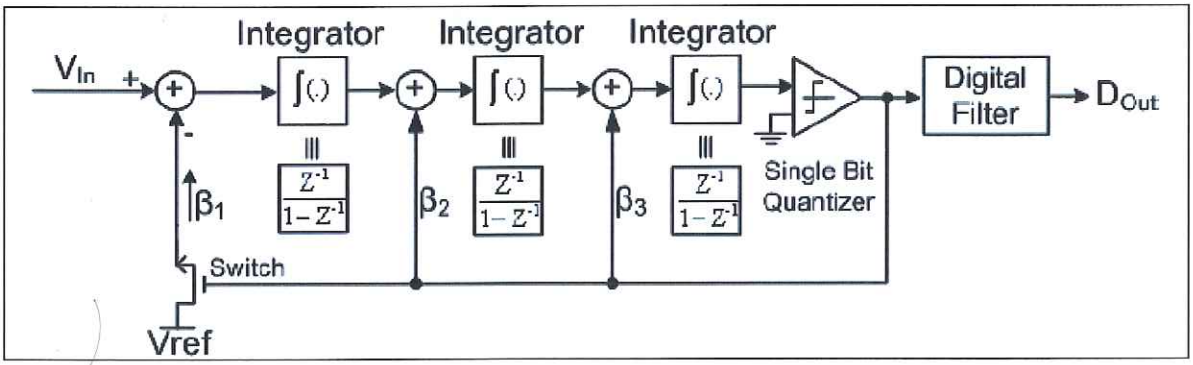
2 b) (Weight 6 %)

Suppose that the S/H should be used for an implant circuit monitoring biological parameters, needing only 6 bits resolution, and receiving signals with maximum frequency components of 500 Hz. What is the sampling time uncertainty that can be tolerated to keep the deviation from the ideal value below 1 LSB?
By how much must the clock jitter improve if the SNR (Signal-to-Noise Ratio) has to be improved by 6 dB?

2 c) (Weight 10 %)

Explain about some important limitations regarding the type of sampling switch used in the S/H circuit in the schematics above.

3 a) (Weight 4 %. Problems 3 a), b) and c) totals 24 % of the exam.)



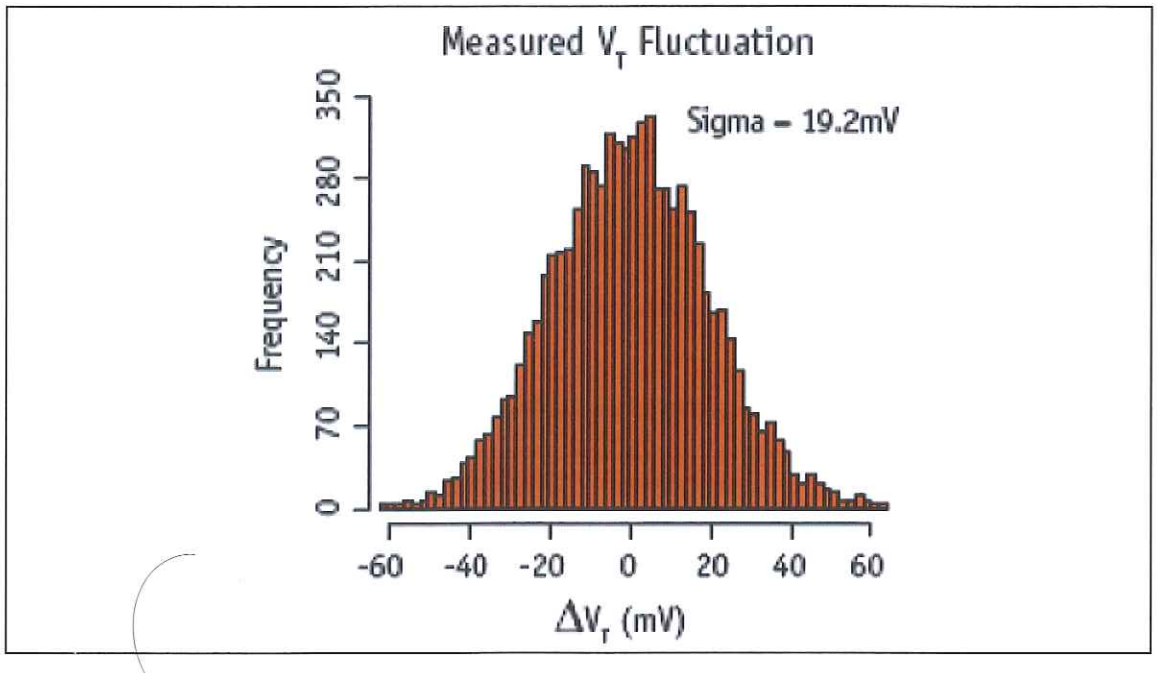
What is the maximum theoretical increase in Signal-to-Noise Ratio ("SNR") when increasing the sampling frequency for the circuit depicted above from f_s to 5 f_s? (Figure taken from: P. Torkzadeh et. al; "*An Elaborate Design and Implementation of a 3rd Order Sigma-Delta Modulator ADC for Wideband Signals*", Proceedings of ICCSC, 2008).

3 b) (Weight 10 %)

A switched-capacitor ("SC") circuit has the following transfer function: $H(z) = V_{out}(z) / V_{in}(z) = C_B / [-(1-z)]C_A$, where C_A and C_B are capacitors and z is related to the z-transform. Draw an SC-implementation of a circuit implementing this H(z). Explain.
Where can such a circuit be useful?

3 c) (Weight 10 %)

For 2nd order noise-shaping, equation 14.32 in "Johns & Martin" expresses $SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log (OSR)$, in [dB]. OSR is the oversampling rate and N is the number of bits. How do you expect the expression for SNR_{max} to change if we had a 3rd order modulator? Explain. You may use relevant assumptions from "Johns & Martin", if you like.



4 a) (Weight 8 %. Problems 1 a), b) and c) totals 24 % of the exam.)

Measured threshold voltage fluctuations in identically drawn MOSFETs, that you for practical assumptions may consider as following a normal "Gaussian" distribution, are shown in the figure above. (The Figure is taken from the article "Characterizing Process Variation in Nanometer CMOS", by Kanak Agarwal, EDA Tech Forum, December 2007.)
Process variations contribute towards variations in theshold voltage and other parameters in active and passive components on chip.
Could you mention some important effects of parameter variations to performance parameters, for CMOS circuits, including some examples?

4 b) (Weight 10 %)

Explain how you may estimate and reduce harmful impacts from parameter variations when doing practical design, during the design process from specifications, via the schematics level to finished layout.

4 c) (Weight 4 %)

Suppose you have a flash ADC with 0.8 V full scale, requiring a comparator offset of maximum $9.47 \cdot 10^{-4}$ V to ensure 99.9 % yield, for a corresponding normal distribution with $\sigma = 3.3$. What is the resolution of the ADC, in number of bits?

5 a) (Weight 9 %. Problems 5 a) and b) totals 10 % of the exam.)

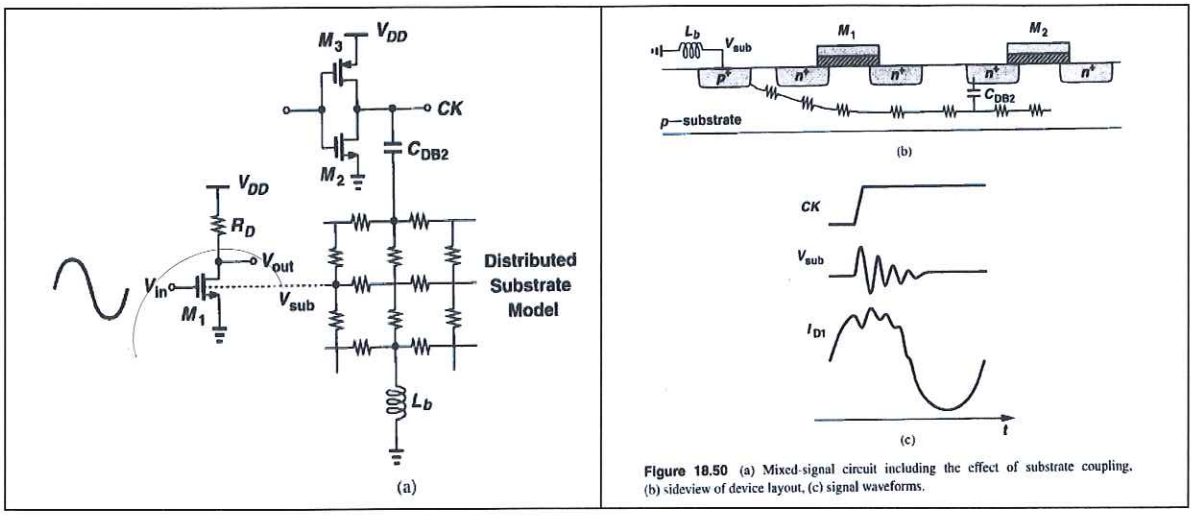


Figure 18.50 (a) Mixed-signal circuit including the effect of substrate coupling. (b) sideview of device layout, (c) signal waveforms.

The Figure above (Fig. 18.50) is taken from "Razavi". Table 2.1 from previously may be used for this problem. Let $(W/L)_1 = 100$ µm/ 0.5 µm, $I_{D1} = 5$ mA and $V_{SB} = 0$. Use a constant gate length of 0.5 µm. If the substrate noise, V_{sub}, has a peak-to-peak amplitude of 50 mV, what is the effect of substrate noise referred to the gate of M_1?

5 b) (Weight 3 %)

The threshold error $\Delta V_{th} = A_{VT} / \sqrt{(WL)}$, according to equation (4.15) in "Maloberti". Increasing the sizing may increase the matching of transistors. Can you mention two qualities of the circuit that are impaired when the product WL increases ?

Good luck!