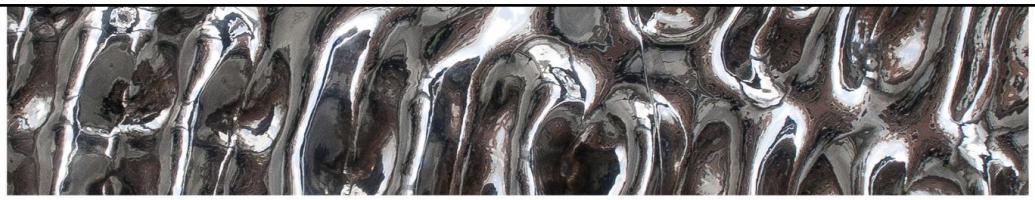


UiO : Department of Informatics
University of Oslo

INF4420

Introduction

Jørgen Andreas Michaelsen

Spring 2013

Outline

- Practical information
- Curriculum overview

Teaching and examination

Lectures (2-3 hours)
Problem solving class (2 hours)
Lab exercises (2 hours)

Final grade:
Exam (60 %)
Project (40 %)

Lectures

Jørgen Andreas Michaelsen
Room: 5405 (OJD, A, 5th floor)
Phone: 22840840
Mobile: 93285523
Email: jorgenam@ifi.uio.no

Lectures Tuesdays 12:15 in OJD 2423, Java

UiO : Department of Informatics
University of Oslo

Problem solving class

Kin Keung Lee (Kody)

Room: 5122

Phone: 22840136

Email: kklee@ifi.uio.no

Assignments for each week (not mandatory)

Fridays 10:15–12:00 in OJD 2465, Prolog

One mandatory assignment

UiO : Department of Informatics
University of Oslo

Labs

Dag Halfdan Bryn

Email: daghb@ifi.uio.no

Weekly labs to learn design tools and work on the project

Thursdays 10:15–12:00. Room TBA.

Webpage

http://www.uio.no/studier/emner/matnat/ifi/INF4420/v13/

Course content

From the course webpage:

"The course provides the know-how and skills needed to design analogue and mixed-signal integrated circuit modules using modern program tools. The main focus of the course is complex systems such as data converters (A/D, D/A) and phase-locked loops (PLL). An introduction is given to CMOS technology and methods in order to implement passive components such as transistors, condensers and coils. In addition, matching, optimisation and noise deflection are all key aspects. The execution of project tasks will be a central part of the teaching."

Learning outcomes

From the course webpage:

"Students will have the skills needed to design an integrated mixed-signal circuit in CMOS using modern design tools."

What is expected of you

The course builds on

- INF3410 (analog, Laplace, freq. response)
- INF3400 (digital, basic transistor, layout)

Please ask questions and give feedback

Integrated circuits

Integrated circuits are “everywhere”

Cost is a driver for new technology. Reduced feature size, smaller dies, CPF decreases, more features on the same die (SoC). Larger wafers.

Reduced feature size helps performance. Is scaling good for analog?

Mixed signal circuits

What are mixed-signal circuits?

Analog + Digital?

Time/Value	Discrete	Continuous
Discrete	Digital	?
Continuous	?	Analog

Why mixed signal?

Digital circuits are more robust and can be designed more systematically. Usually, most of the system and signal processing will be digital content.

We need circuits for regulating supply voltage, clocking, digitizing audio and sensor outputs, communication circuits, etc.

Mixed signal circuits

Digital content dominate. Process development is geared towards reducing cost-per-function (CPF).

Analog and RF functions have to keep up (cost benefits of placing all functions on one die)

→ More than Moore, Through-silicon via

Mixed signal circuits

New ideas to take advantage of new process technology, and new uses of integrated circuits.

Important to have a good understanding of analog and mixed signal circuits. Understand how circuits can be improved and see new possibilities.

Mixed signal circuits

Example:

DALLAS, Aug. 23 /PRNewswire/ -- Texas Instruments Incorporated (TI) (NYSE: TXN) today introduced a dual-channel, single-lane serial-ATA (SATA) redriver and signal conditioner, featuring the lowest active power and lowest automatic low-power (ALP) mode of any 6-Gbps redriver/equalizers available today. The SN75LVCP601 has a maximum active power consumption of 290 mW, or approximately 50 percent less than the nearest competitor, extending critical battery life in portable electronics, such as notebook PCs. ...

Design flow

Top-down design

Specification + different levels of abstraction

Meeting specs across PVT with min power

Usually, big savings are in the architecture

Abstraction

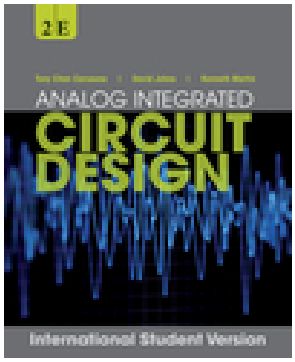
System level (block diagrams, MATLAB)

Schematics (SPICE)

Layout (CAD, DRC, ERC, LVS)

Curriculum

Carusone, Johns, Martin: *Analog Integrated Circuit Design, 2nd Edition International Student Version,* Wiley



http://analogicdesign.com

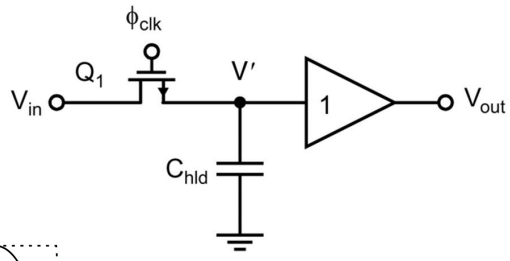
"Second half" of the book.

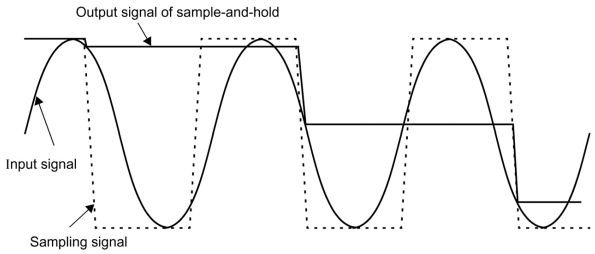
First part covered in INF3410

Sample and hold (Ch 11)

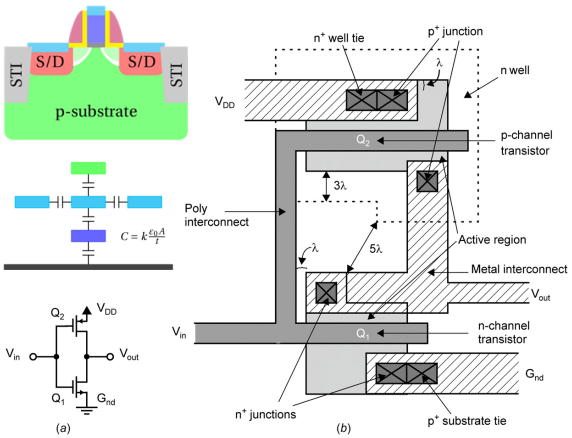
Frontend required in many ADCs.

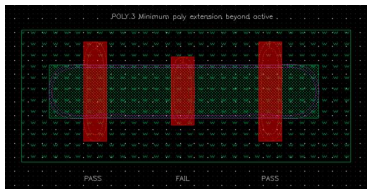
Important for ADC performance.

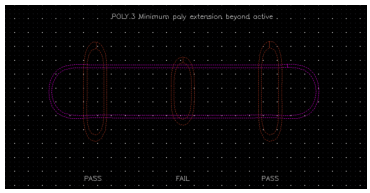




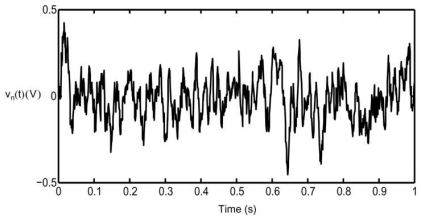
Layout and technology (Ch 2)

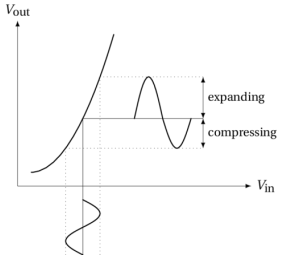






Noise and distortion (Ch 9)

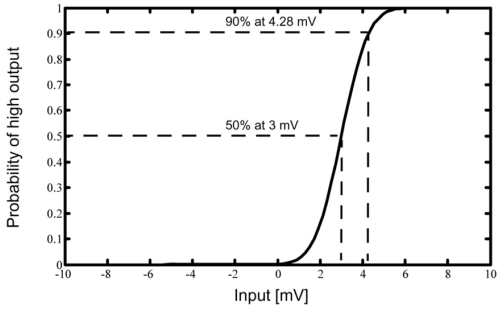


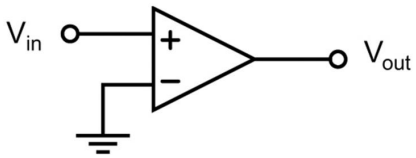


Noise and distortion limits performance.

Comparators (Ch 10)

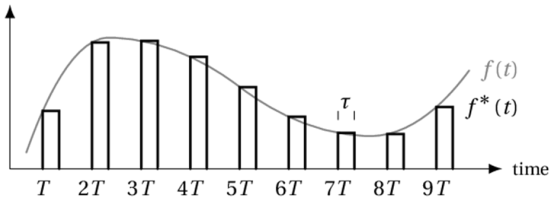
Important building block for ADCs



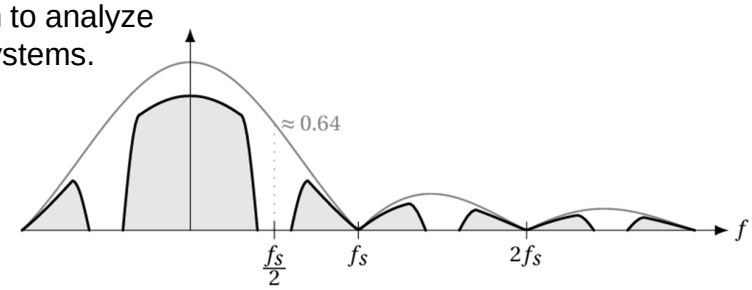


Discrete time (Ch 13)

Important to understand how sampling affects the signal.

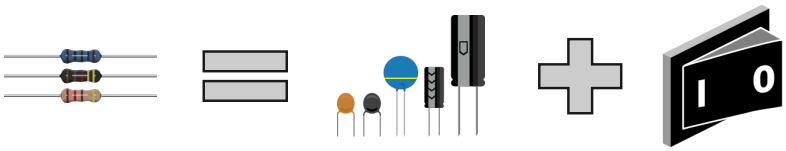


z-transform to analyze sampled systems.



Switched capacitor circuits (Ch 14)

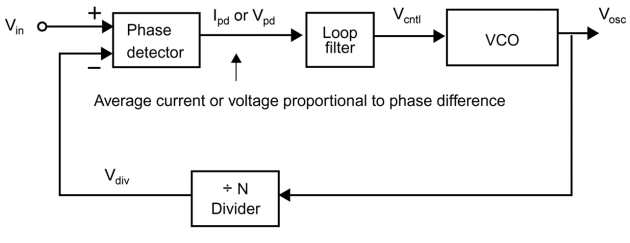
Discrete time analog signal processing

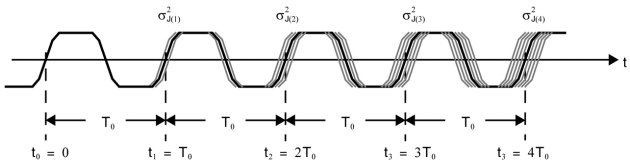


Why?

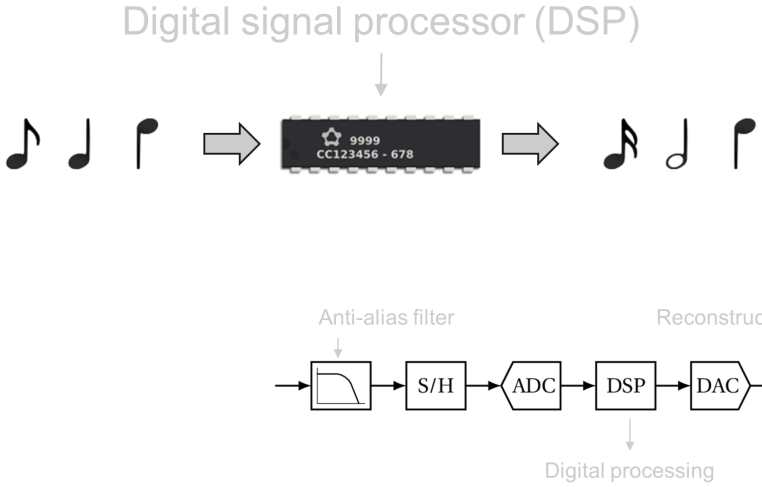
Phase locked loops (Ch 19)

- Frequency multiplication
- Frequency synthesis
- Clock deskew (PLL or DLL)
- Clock recovery (from serial data)
- Demodulation





Data converters (Ch 15–18)



Project

Counts 40 % towards the final grade

Final report is *very* important

Last year: Bandgap + Current steering DAC

This year: Sample and hold circuit

Work in groups of two

Presentation

Process design kit (PDK)

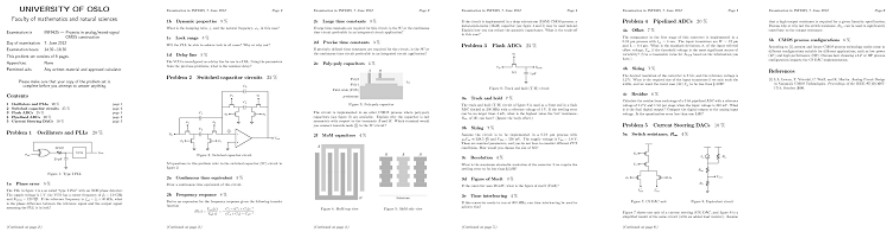
TSMC 90 nm MS/RF LP 1.2 V with 2.5 V I/O
http://www.europractice-ic.com/technologies_TSMC.php?tech_id=90nm

Simulation models
PCells for generating component layout
Rule decks for DRC, ERC, and LVS

NDA is required to access the kit.

Exam

Counts 60 % towards the final grade



Student reference group

- One or two students
- Give feedback on behalf of the students
- Answer questions …