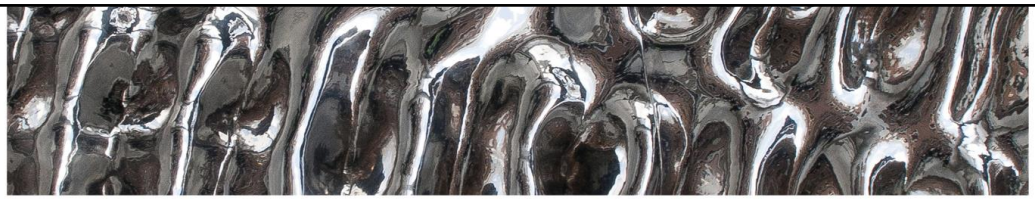

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**INF4420**

# Layout and technology

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## Outline

- CMOS technology
- Design rules
- Analog layout
- Mismatch

## Introduction

As circuit designers we must carefully consider how to draw layout for critical/sensitive parts of the circuit to get **robust** and **predictable** performance. Good simulation results from schematic is not the final answer (but necessary and a good indication).





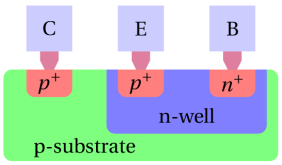
## Introduction

To design circuits that works as intended after manufacturing we must have a basic understanding of how circuits are manufactured, packaged, tested, and how the circuit is used (mounted on a PCB, off-chip parasitic).

## Physical design

The physical circuit is built on a disc of silicon (wafer) layer by layer.

Some layers are implanted in the substrate (front end of line), others layers stacked on top (back end of line)

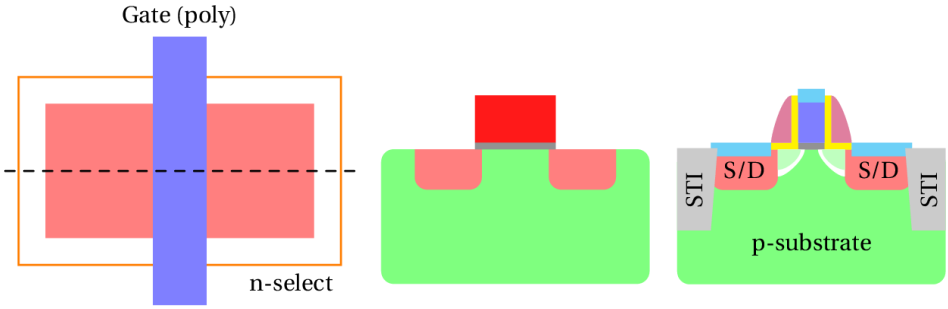







## Physical design

Layout is an encoding of the physical realization of the circuit. But not a 1:1 mapping of what we draw and what the fab puts on the masks.



## Photolithography

Photolithography (litho) is used to transfer the layout to the physical circuit. For each layer.

Light source and mask defines pattern in photoresist. Transferring the image to a physical mask on the wafer.

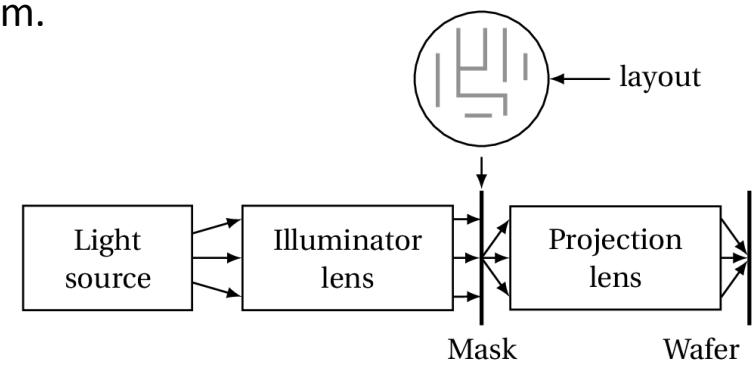






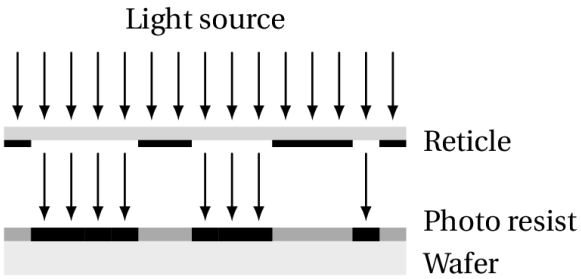
## Lithography system

The layout we create is used to make a mask (or reticle) which is illuminated in the lithography system.



## Lithography system

Photoresist hardens when exposed to light (negative resist), leaving a physical transfer of the mask on the wafer. Rest is removed. Do processing. Rinse and repeat.










## Lithography system

Pattern on wafer is distorted by imperfections in the lithography system.

Wavelength of light is a limitation for feature size.

## Resolution

Resolution is limited by the wavelength of light and numerical aperture (NA) of the lens (given by the angle of light captured by the lens, and the refractive index, *n*)

Resolution: $k_1 \frac{\lambda}{\mathrm{NA}}$

DOF: $k_2 \frac{\lambda}{\mathrm{NA}^2}$

NA: $n \sin \theta$





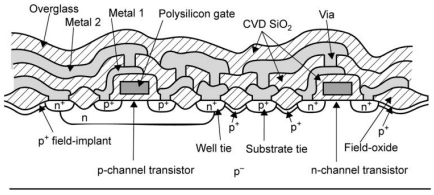


## Depth of focus (DOF)

As the wafer is built layer by layer the geometry becomes uneven.

Wafer is planarized between each step with chemical mechanical polishing (CMP)

inherent tradeoff between DOF and resolution (better NA, finer pitch, more narrow DOF)



## Reducing $k_1$

Optical proximity correction (OPC), sub-resolution assist features (SRAF)








## Reducing $k_1$

- Phase shifting masks (PSM), masks are not binary, but changes the phase of the light.
- Double patterning, split the layout across two (or more) masks.
- Off-axis illumination, optimizing the shape of the light source.

$$\rightarrow k_1 \approx 0.25$$

## Extreme UV

Why not use a light source with extremely short wavelength?

EUV (13.5 nm) in development for a long time, still not used in large scale production. Throughput issues.

Electron beam lithography (e-beam litho) possible but also throughput issues.

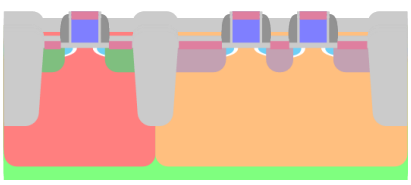




## Front end of line (FEOL)

Process modules that make the active devices

- Active area
- Channel doping
- Gate
- Source/drain extension
- Spacer
- Junction
- Silicide



## Back end of line (BEOL)

BEOL connects the active devices using copper (Cu), separated by low-κ dielectric.

- Pre-metal dielectric (PMD)
- Contacts (source, drain, and gate)
- Inter-level Dielectric (ILD)
- Vias and metal lines



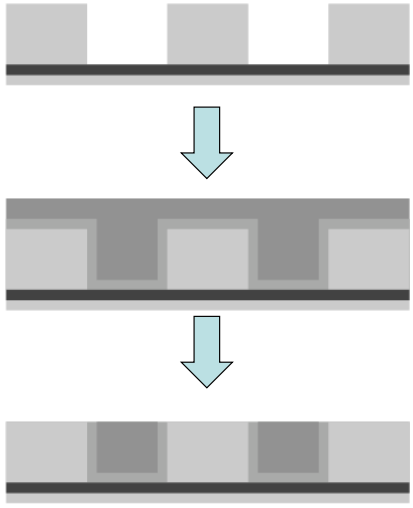




## Dual damascene

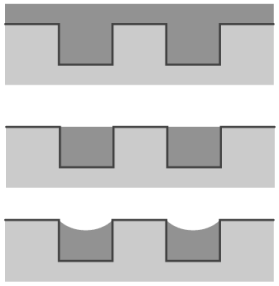
1. Etch trenches in the oxide (barrier).
2. Electroplating adds (excess) copper.
3. CMP to remove the excess copper.

Used for via and lines.

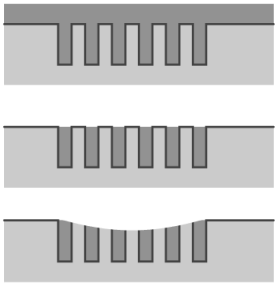


## Dual damascene

Why should we as designers care?



**Dishing** affects
wide metal lines



**Erosion** affects
high density lines





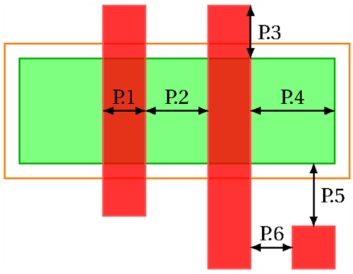
## Design rules

As we have seen, the layout we draw is not perfectly reproduced on the wafer.

We must comply with a set of rules to ensure that the layout we draw is manufacturable. This is a minimum requirement, and does *not* guarantee robust and predictable performance. *Necessary but not sufficient.*

# Design rule examples

| | Rule name (minimum) |
|---|---|
| P.1 | Poly width |
| P.2 | Space poly and active |
| P.3 | Poly ext. beyond active |
| P.4 | Enc. active around gate |
| P.5 | Spc. field poly to active |
| P.6 | Spc. field poly |








# Design rule examples

## Poly rules example (FreePDK45)

| | Rule name (minimum) | Length |
|---|---|---|
| P.1 | Poly width | 50 nm |
| P.2 | Space poly and active | 140 nm |
| P.3 | Poly extension beyond active | 55 nm |
| P.4 | Enclosure active around gate | 70 nm |
| P.5 | Space field poly to active | 50 nm |
| P.6 | Space field poly | 75 nm |

# Design rule examples

## Metal1 rules example (FreePDK45)

| | Rule name (minimum) | Length |
|---|---|---|
| M1.1 | Metal1 width | 65 nm |
| M1.2 | Space metal1 | 65 nm |
| M1.3 | Enclosure around contact (two opposite sides) | 35 nm |
| M1.4 | Enclosure around via1 on two opposite sides | 35 nm |
| M1.5 | Space metal1 wider than 90 nm and longer than 900 nm | 90 nm |
| M1.6 | Space metal1 wider than 270 nm and longer than 300 nm | 270 nm |
| M1.7 | Space metal1 wider than 500 nm and longer than 1.8 um | 500nm |



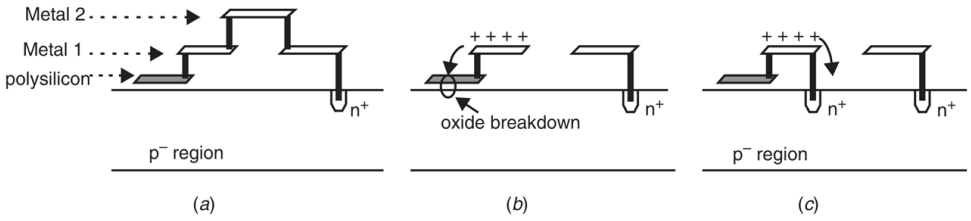


# Density design rules

- Each layer must cover the chip in a specified density.
- Checked inside a “moving” window, e.g. 100 µm × 100 µm.
- Necessary to keep the wafer planar for imaging (DOF limitations)
- Necessary to keep dishing and erosion within limits.
- Automatic dummy filling to comply with density.
- Must be careful with sensitive circuits.

## Antenna design rules

Large metal area connected to a MOSFET gate collects ions during manufacturing and potentially breaks down the gate oxide (irreversibly).





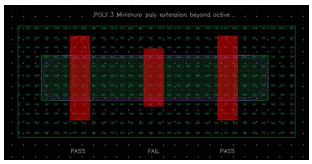


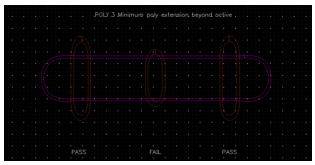

## Design rule check (DRC)

- Large number of rules, difficult to keep track of
- Tool to check design rules, DRC
- Foundry provides rule set as part of the PDK
- Pass / fail vs. levels of severity
- Default DRC rules are “minimum”
- Foundry usually also provides rules for analog and sensitive circuits.

## Litho friendly design (LFD)

- Design rules does not guarantee a robust design or good yield
- Design for manufacturability (DFM) tools simulate and analyze how the layout will print
- Difficult to get access to data / rules.








## Layout vs. schematics (LVS)

- Compare layout to schematics
- Make sure the layout performs the function we intended
- Recognizes shapes in the layout (e.g. transistors) and how they are connected.
- Foundry provides rules for recognizing devices as part of the PDK

## Post layout simulation

- Schematic level simulates devices based on assumptions of how they are drawn
- Parasitics and non-ideal effects depends on how we draw the layout
- Some of these effects can be automatically extracted → more accurate simulation results
- Parasitics also have temperature dependence, corners, etc.
- Slow! Many components are added.

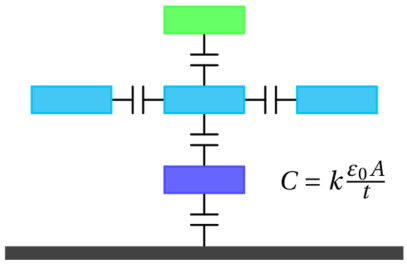




## Interconnect parasitics

Overlap capacitance

Low-κ dielectric helps reduce interconnect capacitance.




Fringe capacitance also important.

## Interconnect parasitics

Consider resistance and capacitance (and inductance).

Typical metal resistance is 0.1 Ω/□
10 Ω per via (never use one single via)

Current handling capability (electromigration)

Process documentation lists actual values





## Interconnect parasitics

Sizing metal lines is a trade-off between capacitance and resistance (and current handling capability)

Wide lines, fewer squares, less resistance, but potentially more overlap capacitance.

Resistance and capacitance vary due to dishing and erosion.

## Passive components

Need passive components (resistors, capacitors) for analog and mixed signal circuits. (RF needs inductors).

Process tries to minimize resistance and capacitance. Components become impractically large.

Process options for passive components.





## Resistors

Several possibilities. Need to consider:

- Ω/☐ (area, practical limit for large R)
- Temperature dependence (TC)
- Voltage dependence (linearity)
- Mismatch (ΔR/R, abs value +/- 20 %)
- Parasitic capacitance

The TC and voltage dependence is not only linear, but also quadratic in the simulator.
E.g. R(T) = R(T0) [1 + TC1(T-T0) + TC2(T-T0)^2]. Similar for voltage dependency.

## Resistors

Realistic alternatives for large resistors

N-well: Large R, poor TC (> 2000 ppm/C), poor linearity (< 1 %), low mismatch, parasitic capacitance from pn-depletion. Always available.

Poly with silicide block: Large R, good TC (~ 100 ppm/C), reasonable linearity (< 0.1 %), low mismatch. Extra layer needed.





## Capacitors

Need to consider

- F/m^2
- Temperature dependence (TC)
- Voltage dependence (linearity)
- Mismatch (ΔR/R)
- Cost

## Capacitors

MOSCAP, using gate capacitance as a capacitor. Very high capacitance per unit area, non-linear, useful for decoupling, but gate leakage current is problematic.

PiP (poly-insulator-poly), using two poly layers. Usually not available in modern CMOS.



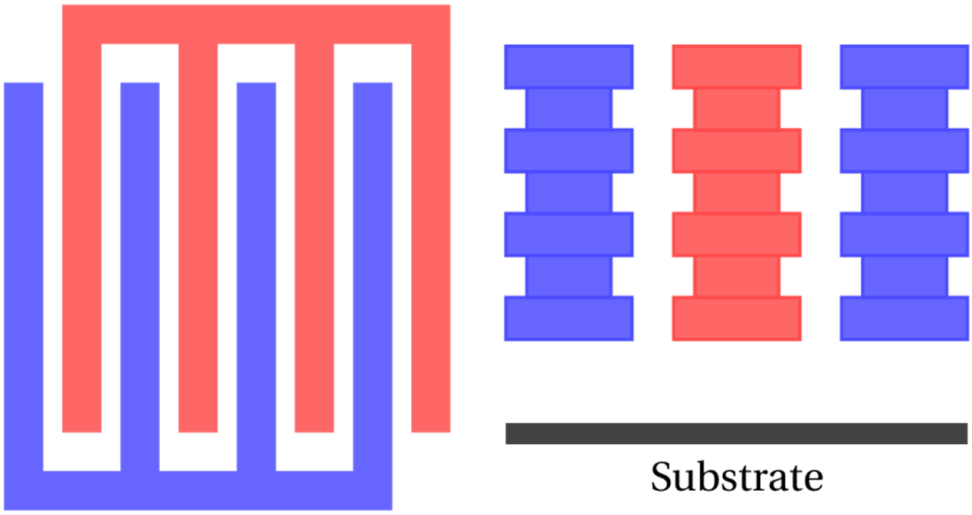


## Capacitors

MiM (metal-insulator-metal). Extra masks required. About 1 or few $\frac{\mathrm{fF}}{\mathrm{um}^2}$. Good option if available. Thin separation of (high) metal layers with special dielectric.

MoM (metal-oxide-metal). Exploit fine pitch in CMOS. No process option required.

## MoM capacitors










## Matching passive components

Systematic vs. random

- Absolute component value changes between runs
- Layout dependent issues
- Stress, thermal, or doping gradients
- Random difference between two identically drawn matched components

## Matching passive components

We want to minimize the systematic variation for critical components. How can we make sure two capacitors are equal, or $C_2 = n \times C_1$? (There will still be (small) random differences)

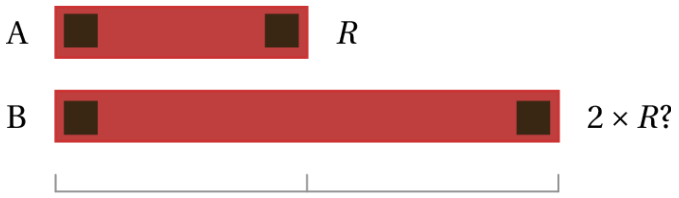
- Unit elements
- Dummies
- Interdigitation or common centroid







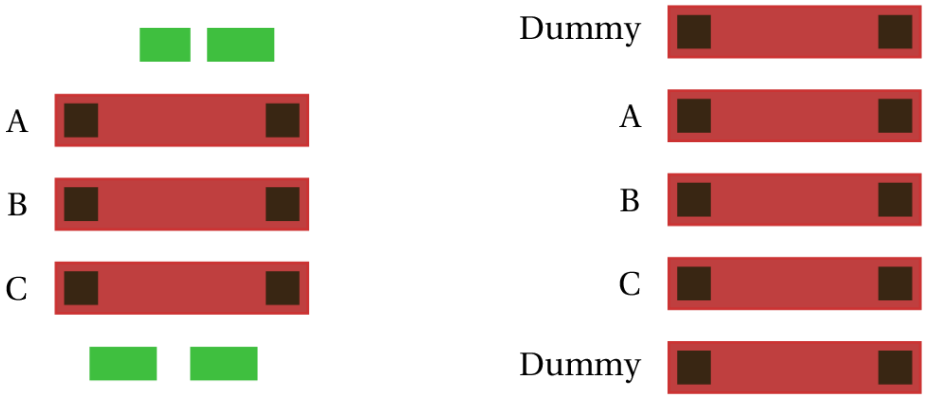
## Unit elements




Instead, make *identical* unit elements.

## Dummy elements

Make sure matched elements see the *exact* same surroundings










## Interdigitated layout


Process gradient almost evenly distributed between components A and B.

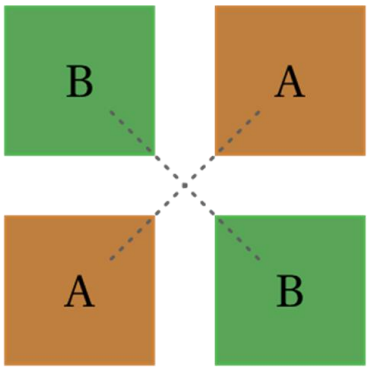
A and B are split into units

## Common centroid

Perfect cancelation of linear gradients.

Several patterns are possible.

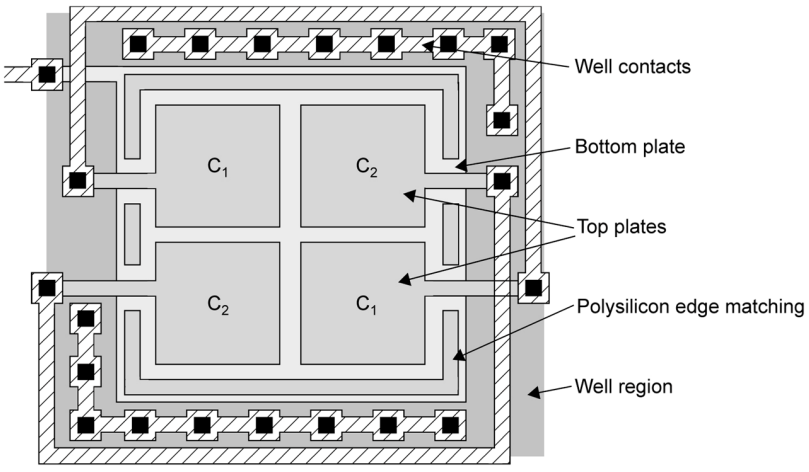
Can split A and B into more than two units.



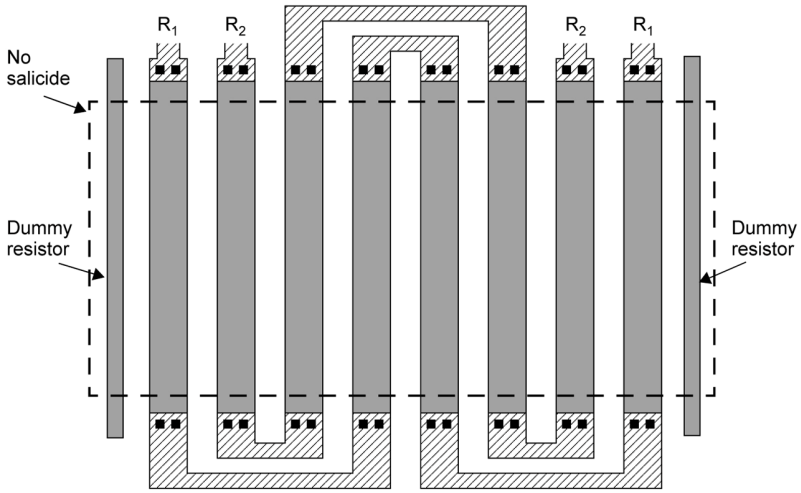





## Capacitor layout example



# Resistor layout example







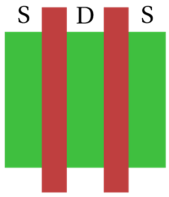

# Drawing transistors

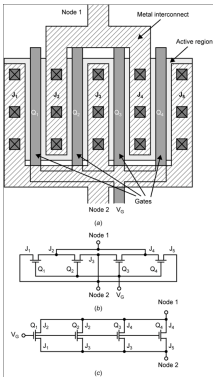
So far we have discussed passive components. The same rules apply for transistors. But there are more issues with transistors …

- Multi-finger devices
- S/D symmetry
- WPE and LOD

## Multi-finger devices

Less drain capacitance, less gate resistance. Set this in schematics to model correctly!

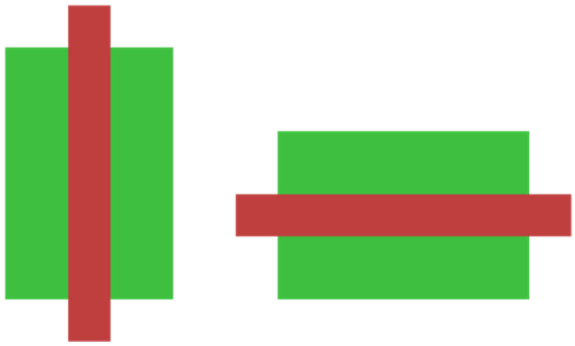





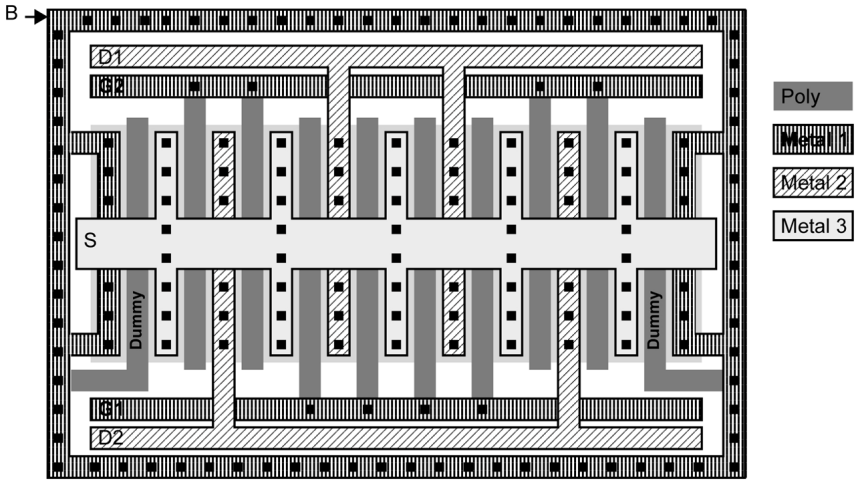



## Device orientation

Devices with different orientation do not match!



# Diff pair layout example



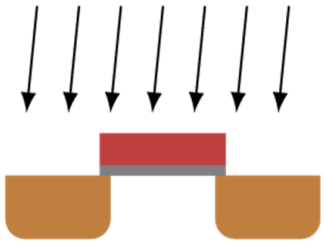







# Source/drain asymmetry

Source and drain may be asymmetric due to ion implantation angle. (Angle is necessary to avoid implant depth issues, channeling.)



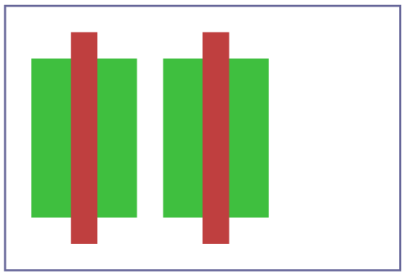
## Well proximity effect (WPE)

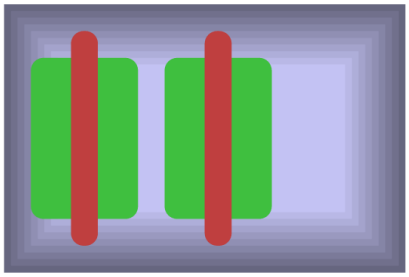
High energy ion implants to form the well. Scattering from the edge of the photoresist mask, and embedding in the silicon surface (near well edge). Transistors close to the well edge will therefore have different properties. This is known as the well proximity effect (WPE). Important for matching.





## Well proximity effect (WPE)





As with S/D asymmetry, implantation angle may render the scattering and doping asymmetric.

Affects threshold voltage, body effect, and mobility.

## STI stress (LOD)

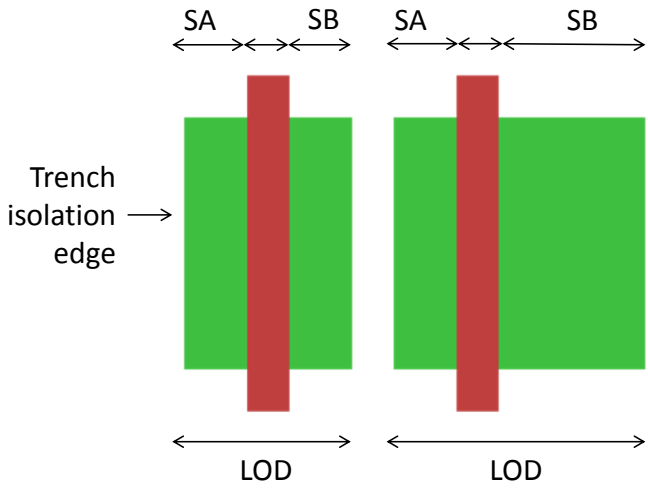
Shallow trench isolation strains the active area of the transistor. Influences mobility and threshold voltage (stress induced enhancement or suppression of dopant diffusion). Distance between gate and STI impacts performance. Important for matching. (Parameters SA and SB in BSIM). Also known as LOD (length of diffusion),

LOD = SA + SB + L. SD for distance between fingers in multifinger device.



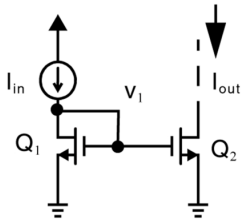


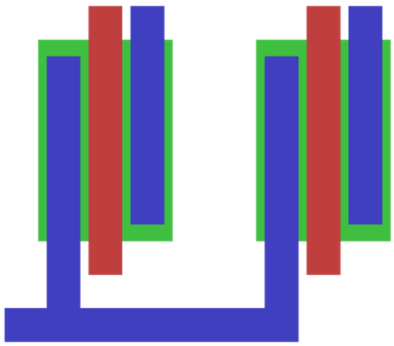
## STI stress (LOD)



## Transistor interconnect

Unbalanced metal routing: Transistors see different source voltage.



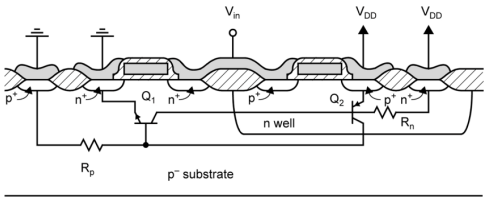
**Distribute references as *currents*, not bias voltage.**

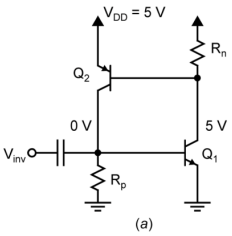




## Latch-up

Parasitic bipolar transistors may inadvertently turn on and “latch”. Large current flows.

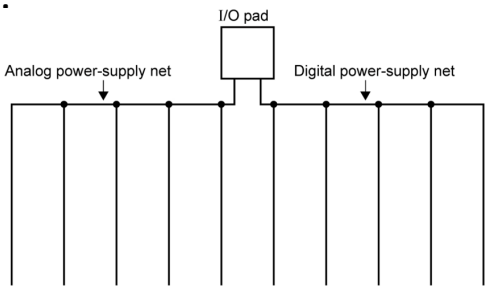


## Power supply noise

Separate the analog and digital supply nets as close to the source as possible (preferably off-chip). Decoupling. PSRR.

- Finite impedance in the supply nets
- Bond wire inductance

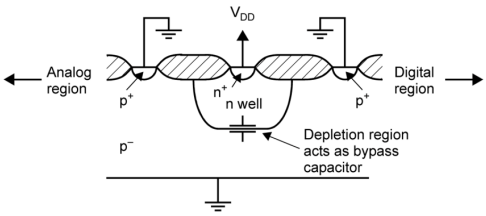







## Substrate noise coupling

Drain current also depends on bulk potential. Digital switching couples to analog circuits through the bulk. Separation and shielding (with deep n-well where available). Separate pin for the guard ring.



## Mismatch

Previously we have discussed systematic mismatch. Systematic mismatch can be minimized by careful layout or trimming. Binning is also used.

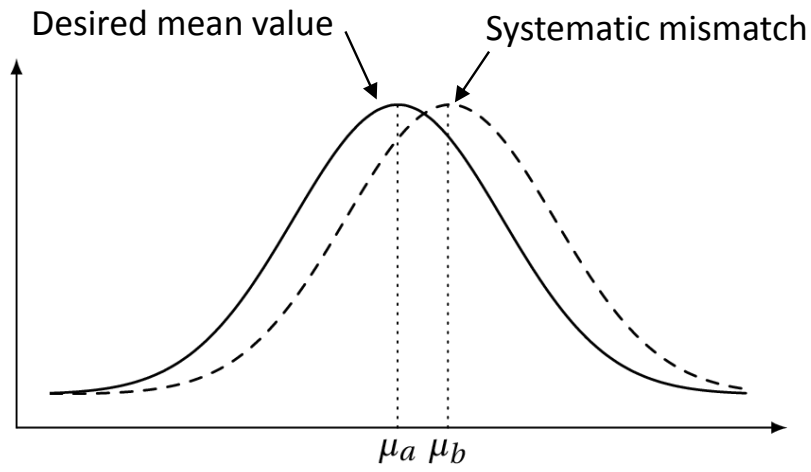
When "identical" devices are manufactured, random fluctuations cause electrical parameters of devices on the same die to have a statistical distribution—Random mismatch.





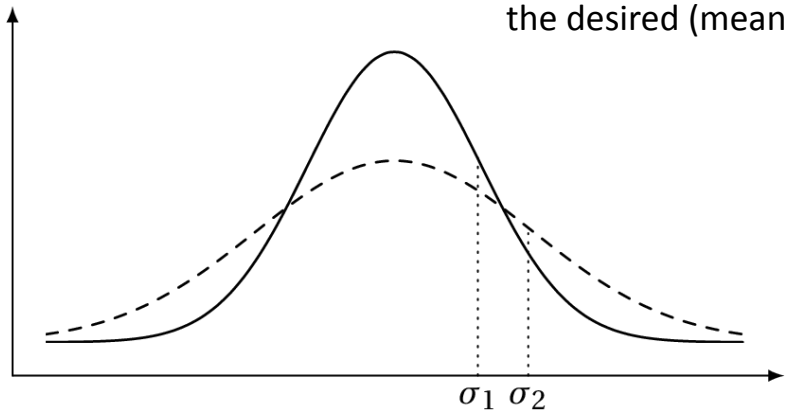


## Systematic mismatch



## Random mismatch

Better = more devices will be closer to the desired (mean) value










## Worst-case analysis

Assuming a normal distribution (reasonable assumption from the central limit theorem)

Worst case minimum value: $\mu - 3\sigma$

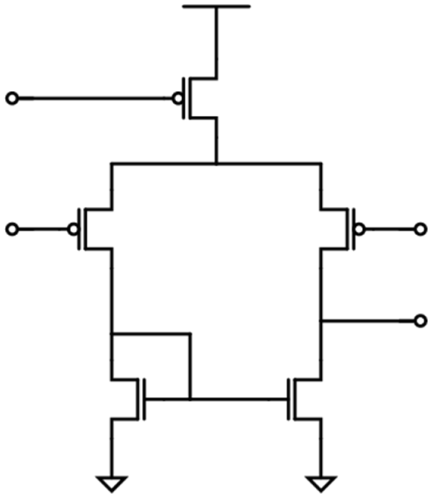
Worst case maximum value: $\mu + 3\sigma$

$3\sigma$ is 99.73 %

$6\sigma$ is 99.9999998 %

## Matching

- Need matching in input pair and current mirror
- Systematic and random

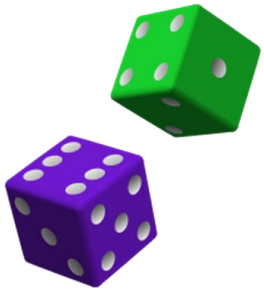






## Monte-carlo simulation

- Fab provides statistical parameters for the device models
- Simulator can run a number of simulations with different permutations of the parameters
- Does not necessarily tell us where the problem is



## Hand calculation of matching

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 24, NO. 5, OCTOBER 1989 1433

Matching Properties of MOS Transistors

MARCEL J. M. PELGROM, MEMBER, IEEE, AAD C. J. DUINMAIJER, AND ANTON P. G. WELBERS

$$\sigma^2_{\Delta P} = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

A systematic study of mismatch between parameters of two identical MOSFETs.





## Hand calculation of matching

Matching of parameter, P, between two identically drawn devices

Parameters of devices closely spaced exhibit a random variance **inversely proportional to area**.

Area proportionality constant

$$\sigma^2_{\Delta P} = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

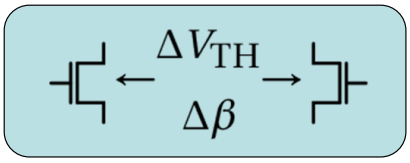
Distance

Size

Variation with spacing

## Hand calculation of matching

Mismatch between *two* identically drawn adjacent transistors. We use the previous formula to find $\Delta V_{\mathrm{th}}$ and $\frac{\Delta\beta}{\beta}$. Then we use these results to find $\frac{\Delta I_D}{I_D}$, $V_{\mathrm{OS}}$, etc.




$$I_D = \frac{\mu_n C_{\mathrm{ox}}}{2}\frac{W}{L}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)^2 = \frac{\beta}{2}\left(V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)^2$$





## Sources of randomness

- Line edge roughness (LER)
- Random dopant fluctuation (RDR)
- Gate oxide thickness
- …

Some effects due to the manufacturing process may not be truly random, but will appear random to us as designers, because it's outside our control. We will count this as "random".

# Line edge roughness (LER)

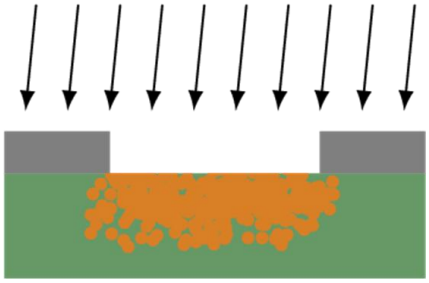
*"LER is caused by a number of statistically fluctuating effects at these small dimensions such as shot noise (photon flux variations), statistical distributions of chemical species in the resist such as photoacid generators, the random walk nature of acid diffusion during chemical amplification, and the nonzero size of resist polymers being dissolved during development. It is unclear which process or processes dominate in their contribution to LER."*
[http://spie.org/x32401.xml]





# Random dopant fluctuation

As features scale, fewer dopant atoms in the channel. The relative contribution of one atom increases. Single atom affects electrical parameters.



## Threshold voltage mismatch

Important contributions are oxide thickness ($t_{\mathrm{OX}}$) and dopant concentration in the channel region.

Improves with scaling in $t_{\mathrm{OX}}$.

Standard deviation of the absolute threshold voltage difference

$$\sigma_{\Delta \mathrm{VTH}} = \frac{A_{\mathrm{VTH}}}{\sqrt{WL}}$$

Technology parameter

Best guess

$$\frac{A_{\mathrm{VTH}}}{t_{\mathrm{ox}}} \approx \frac{\mathrm{mV} \cdot \mu\mathrm{m}}{\mathrm{nm}}$$





## $\beta$ (current factor) mismatch

Relative current factor mismatch, $\frac{\Delta\beta}{\beta}$ [%].

$$\frac{\sigma^2_{\Delta\beta}}{\beta^2} = \frac{A^2_\mu}{WL} + \frac{A^2_{\mathrm{COX}}}{WL} + \frac{A^2_W}{W^2L} + \frac{A^2_L}{WL^2} \approx \frac{A^2_\beta}{WL}$$

Beta guess for $A_\beta$ is 2 % µm

# Drain current mismatch

$$I_D = \frac{\beta}{2}(V_{GS} - V_{TH})^2$$

We know the standard deviation of $\beta$ and $V_{TH}$, and

$$\sigma_y^2 \approx \left(\frac{\partial y}{\partial x_1}\right)^2 \sigma_{x_1}^2 + \left(\frac{\partial y}{\partial x_2}\right)^2 \sigma_{x_2}^2 + \cdots + \left(\frac{\partial y}{\partial x_n}\right)^2 \sigma_{x_n}^2$$

$$\frac{\sigma_{\Delta I_D}^2}{I_D^2} = \frac{4\sigma_{\Delta V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_{\Delta\beta}^2}{\beta^2} = \left(\frac{g_m}{I_D}\right)^2 \sigma_{\Delta V_{TH}}^2 + \frac{\sigma_{\Delta\beta}^2}{\beta^2}$$

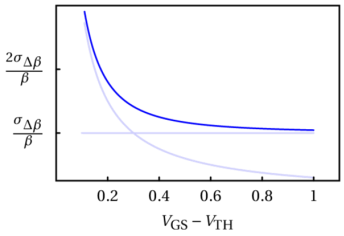


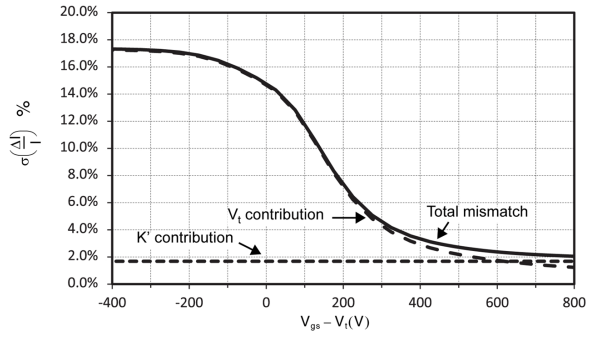


# Drain current mismatch

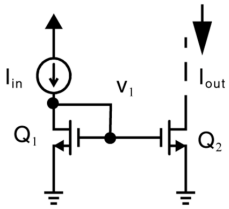
$$\frac{\sigma_{\Delta I_D}^2}{I_D^2} = \frac{4\sigma_{\Delta V_{TH}}^2}{(V_{GS} - V_{TH})^2} + \frac{\sigma_{\Delta\beta}^2}{\beta^2} = \left(\frac{g_m}{I_D}\right)^2 \sigma_{\Delta V_{TH}}^2 + \frac{\sigma_{\Delta\beta}^2}{\beta^2}$$

$$A_{VT} = 4\ \text{mV}\ \mu\text{m}, A_\beta = 1\ \%\ \mu\text{m}, \frac{W}{L} = \frac{2\ \mu\text{m}}{0.2\ \mu\text{m}}$$



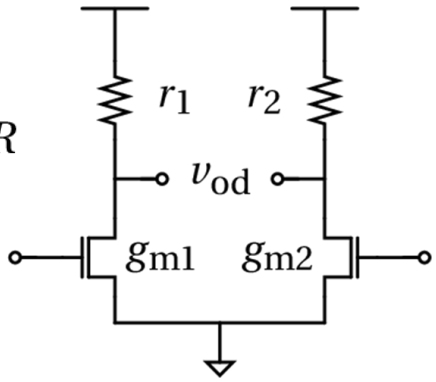

*One* standard deviation



# Input referred offset

$$\sigma_{\mathrm{VOS,out}} = \sigma_{\Delta I_D} \cdot R,\ A_0 = g_m R$$

$$\sigma_{\mathrm{VOS,in}} = \frac{\sigma_{\mathrm{VOS,out}}}{A_0} = \frac{\sigma_{\Delta I_D}}{g_m}$$




$$\sigma^2_{\mathrm{VOS,in}} = \sigma^2_{\Delta \mathrm{VTH}} + \frac{(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2}{4} \frac{\sigma^2_{\Delta\beta}}{\beta^2}$$





# Some basic rules for drawing layout

- Drawing layout is not like drawing schematics (at all). The GUI looks similar, but this is where the similarity ends.
- Start thinking about the layout when doing the schematics. Think about how this schematic translates to the layout (is it practical to common centroid this if needed). Number of fingers, DFM and analog options, etc.
- Check DRC often. Avoids having to change “everything” later.
- Use hierarchies and unit cells. Make sure the addition at each level is small enough to be manageable.
- Make sure each unit cell passes LVS. If layout is large, LVS gets confused when (not if) you make mistakes.

## Some basic rules for drawing layout (cont.)

- The MOS transistor is a four terminal device. Bulk contacts!
- Layout XL is not necessarily a better option. It does not know that you want to interdigitate two resistors. Nor does it care about dummies. Again, layout is not another schematics. Work on small unit cells and hierarchies to keep track of the design instead.
- Doing layout efficiently takes practice. Expect to spend a lot of time drawing and fixing errors from DRC and LVS.
- There are a number of options for parasitic extraction. E.g. is the nwell extracted with the junction diode? Usually configurable. You have to know the level of detail to get accurate results.
- The actual circuit is in 3D (CAD shows 2D view). Think about how things look in the physical circuit.





## Further reading

- BSIM Manual (LOD ch 13, WPE ch 14)
- Hastings, *The Art of Analog Layout*, Prentice Hall, 2001
- Pelgrom, *Component matching: best practices and fundamental limits*, IDESA.
- Skotnicki, et. al., *Innovative Materials, Devices, and CMOS Technologies for Low-Power Mobile Multimedia,* IEEE Trans. Electron Devices, 55 (1).