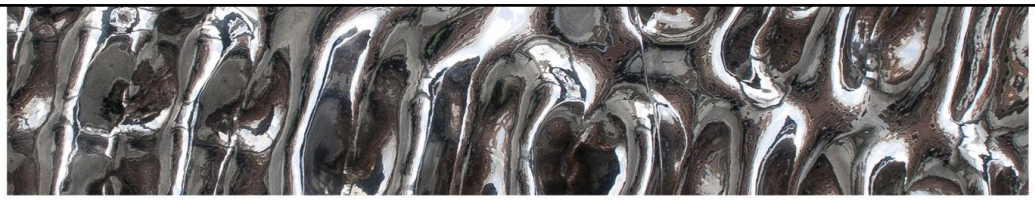


UiO : Department of Informatics
University of Oslo

INF4420

Switched-Capacitor Circuits

Jørgen Andreas Michaelsen

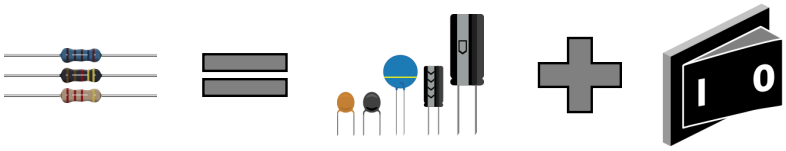
Spring 2013

Outline

- Introduction (why and how)
- Integrators and filters
- Gain circuits
- Noise and charge injection

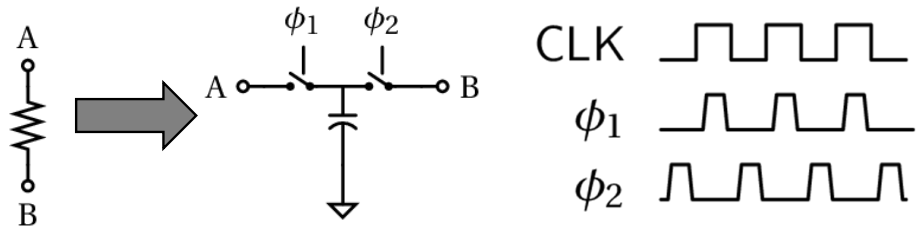
Introduction

Discrete time analog signal processing



Why?

Introduction



The arrangement of switches and the capacitor approximates a resistor.

Introduction

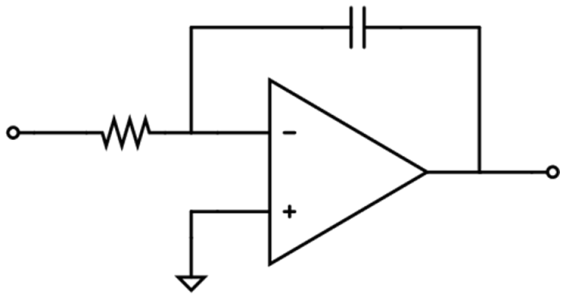
Assuming steady-state, and arbitrarily assume $V_A > V_B$, T is one clock cycle.

1. At the *beginning* of ϕ_1, the capacitor voltage, V_C, is at V_B Volt
2. During ϕ_1, the capacitor is charged to V_A. The charge transferred to the capacitor during ϕ_1 is $\Delta Q = C(V_A - V_B)$
3. During ϕ_2, ΔQ is transferred from the capacitor to B

There is a net charge transfer, ΔQ, from A to B every period. This approximates a resistor, but the charge transfer is discrete.

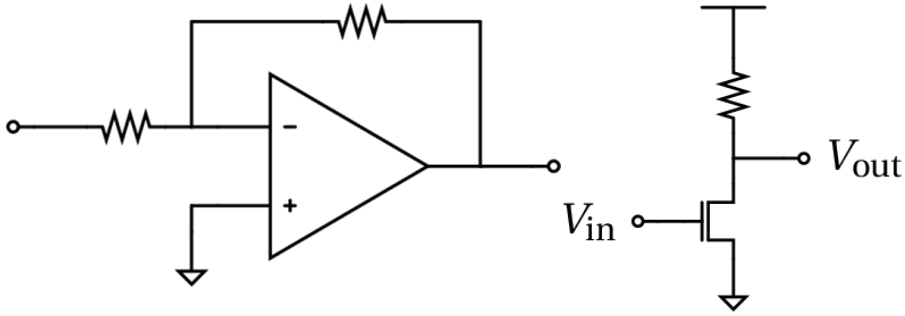
$$\overline{I} = C\frac{V_A - V_B}{T} \rightarrow \overline{R_{eq}} = \frac{T}{C}$$

Introduction



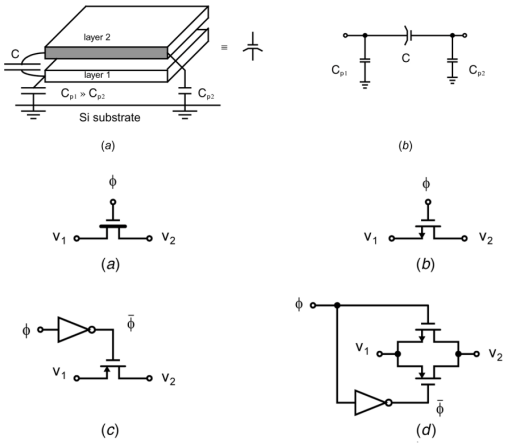
RC accuracy (matching). Large time constants implies large passive components. With SC the time constant is set by capacitor ratio and clock frequency (both precisely controlled).

Introduction

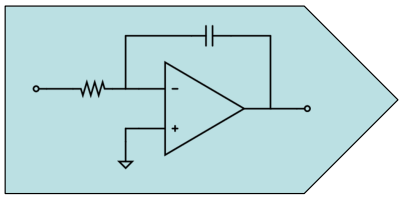


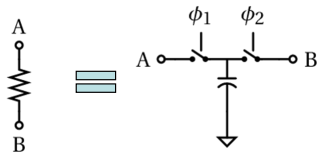
Resistive loading is undesirable in CMOS. Small-signal gain: $g_m r_o$. When loaded with a resistor, r_l, the gain is $g_m(r_o||r_l)$. I.e. the gain decreases.

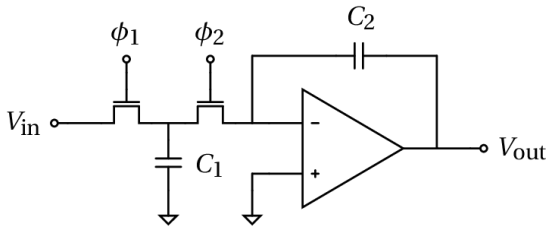
Building blocks



Integrators

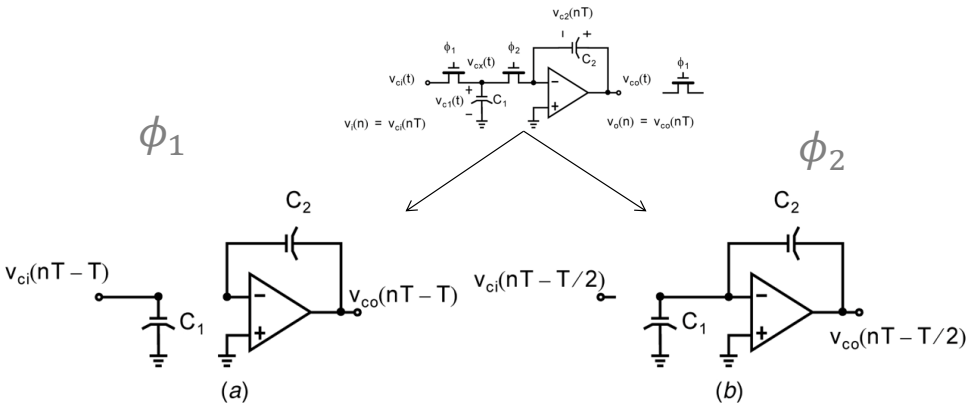






Discrete integrators

Analyze each clock phase separately



Discrete integrators

Analyzing the charge transfer results in

$$H(z) = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} = -\frac{C_1}{C_2}\frac{1}{z-1}$$

(Describes the output sampled at the end of ϕ_1)

Delaying integrator (as we are multiplying with z^{-1}) or equivalently from the time domain equation, the output "now" is given by the "previous" output and the "previous" input.

Discrete integrators

From the z-domain transfer function we find the frequency response.

Assume the input frequency is $\ll T^{-1}$, we have

$$H\left(e^{j\omega T}\right) \approx H(1+j\omega T) = -\frac{C_1}{C_2}\frac{1}{j\omega T}$$

Compare to the continuous time case,

$H(j\omega) = \frac{1}{\mathrm{j}\omega RC} = \frac{1}{\mathrm{j}\omega\tau}$, gives discrete time,

Discrete time time constant

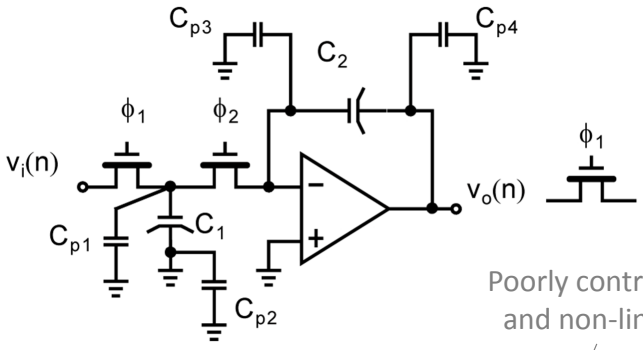
$$\tau = \frac{C_1}{C_2}\frac{1}{T}$$

Discrete integrators

The discrete time equivalent time constant is defined by the capacitor ratio and clock frequency.

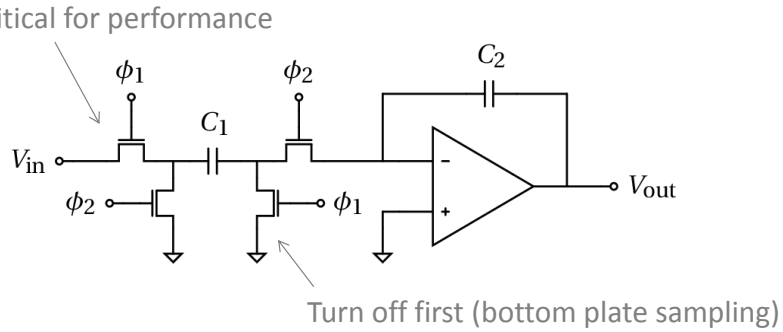
- Allows precise time constant definition.
- Allows large time constants without excessively large passive components.

Integrator parasitic capacitance



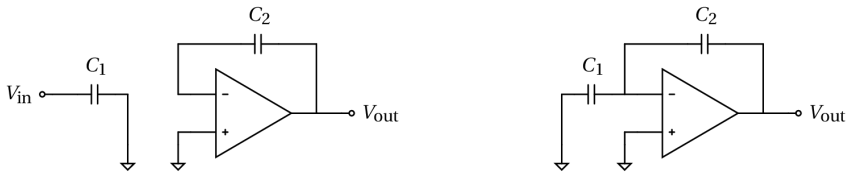
$$H(s) = -\frac{C_1}{C_2}\frac{1}{z-1} \rightarrow -\frac{C_1 + C_{p1}}{C_2}\frac{1}{z-1}$$

Parasitic insensitive integrators



Again, we analyze the charge transfer from one clock phase to the next to find the transfer function.

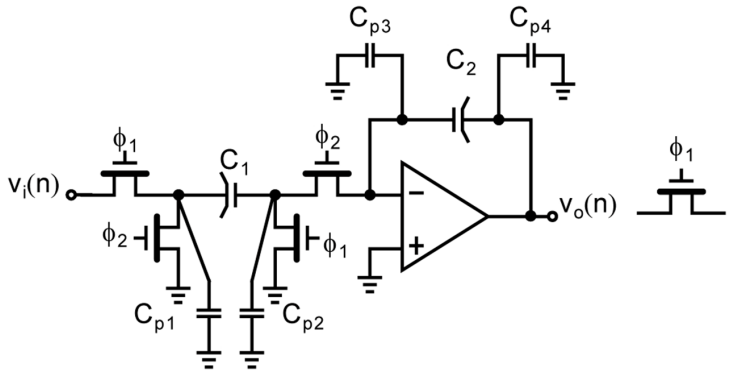
Parasitic insensitive integrators



Almost the same as before (delaying integrator), but the added switches flips the capacitor → positive gain.

$$H(z) = \frac{C_1}{C_2}\frac{1}{z-1}$$

Parasitic insensitive integrators



The parasitic capacitors still affect settling, but not the signal charge transfer.

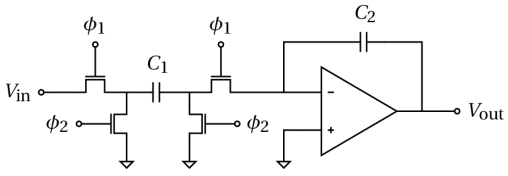
Delay free integrator

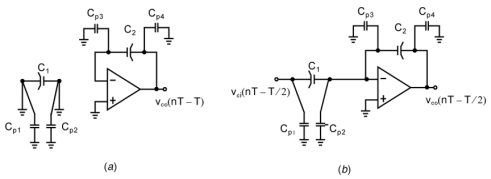
Same circuit as before, but modified clocking of the switches.

$$C_2 v_o(nT) = C_2 v_o\left(nT - \frac{T}{2}\right) - C_1 v_i(nT)$$
$$= C_2 v_o(nT - T) - C_1 v_i(nT)$$

$$v_o[n] = v_o[n-1] - \frac{C_1}{C_2} v_i[n]$$

$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2}\frac{1}{1 - z^{-1}}$$
$$= -\frac{C_1}{C_2}\frac{z}{z - 1}$$





Signal flow graph analysis

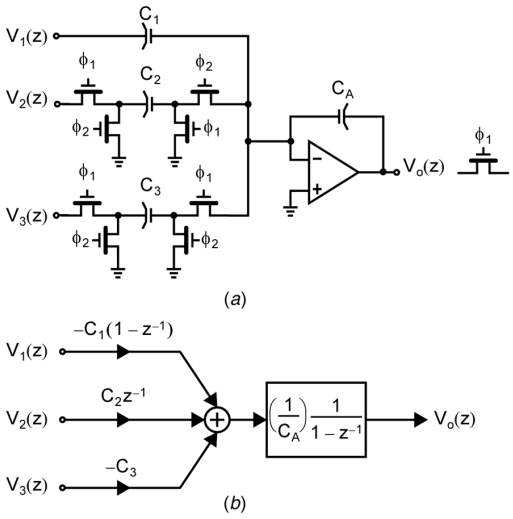
- Now we have the fundamental building blocks (discrete time integrators), to realize filters.
- We need a more convenient tool to analyze large systems.
- Signal flow graph (SFG) analysis allows us to graphically analyze SC systems.

Signal flow graph analysis

$H_1(z) = \frac{V_o(z)}{V_1(z)} = -\frac{C_1}{C_A}$
(inverting gain stage)

$H_2(z)$ is the non-inverting delaying integrator

$H_3(z)$ is the inverting delay-free integrator



SC filters

A simple design strategy:

- Start with a continuous time prototype
- Replace resistors with SC resistor equivalents

The resulting circuit is similar for input frequencies much lower than the sampling frequency

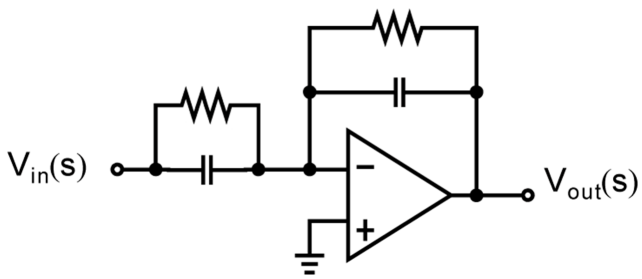
- Use SFG to determine the *z*-domain transfer function

Accurate description of the transfer function

First order filters

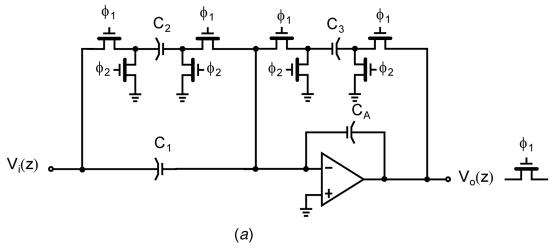
Filter design example.

Start with the continuous time circuit. In this case:

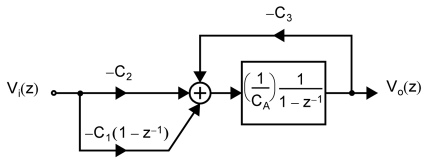


First order filters

Replace the resistors with SC elements



(a)



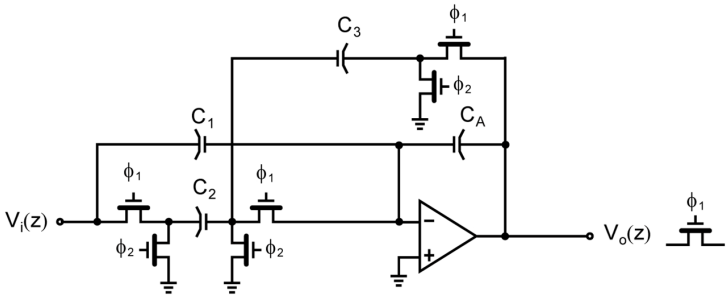
(b)

First order filters

- Use Fig. 14.14 to find the SFG
- From this we find the *z*-domain transfer function
- $H(z) = -\frac{1}{C_A}\frac{C_2+C_1\left(1-z^{-1}\right)}{1+\frac{C_3}{C_A}-z^{-1}}$
- Find pole and zero (stability)
- Frequency response, $z = e^{j\omega T} \approx 1 + j\omega T$

Switch sharing

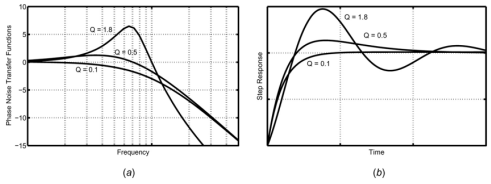
Some switches are redundant, we use this to simplify the circuit:



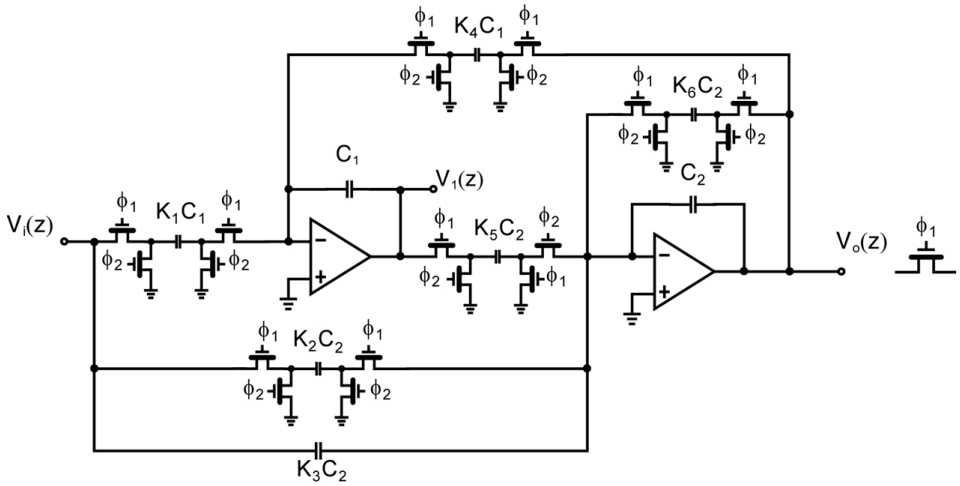
Biquad filters

Ratio of two quadratic functions. In continuous time

$$H(s) = -\frac{k_2 s^2 + k_1 s + k_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}$$

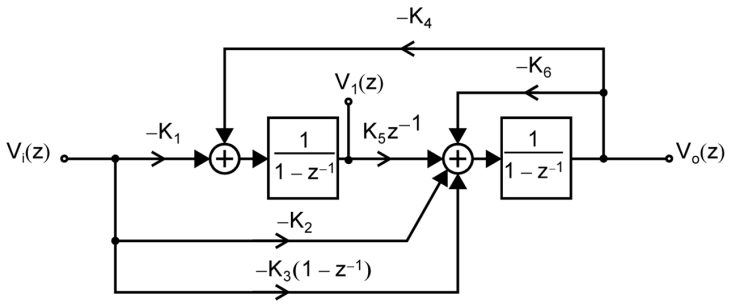


Low-Q biquad



Low-Q biquad

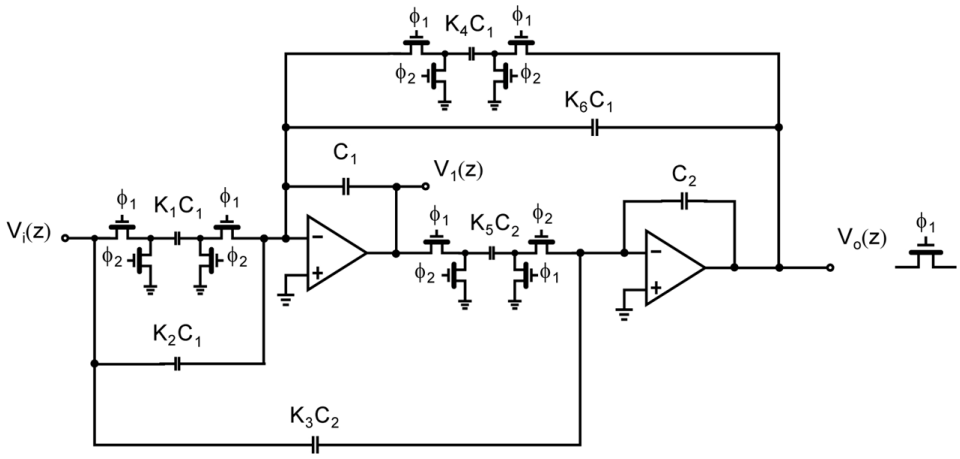
$$H(z) = -\frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1}$$



Low-Q biquad

- A design strategy for determining capacitor sizing is outlined in the book
- High-Q transfer functions result in large capacitor spread (ratio of the smallest and largest capacitor)
- As before, we find the frequency response as $H\left(e^{j\omega T}\right)$

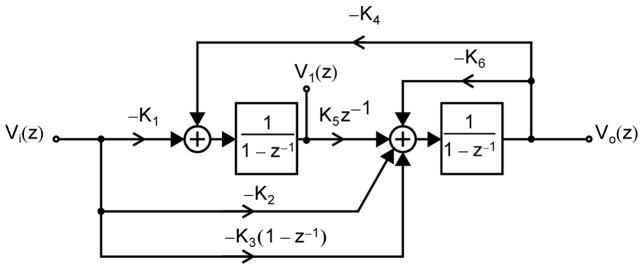
High-Q biquad



High-Q biquad

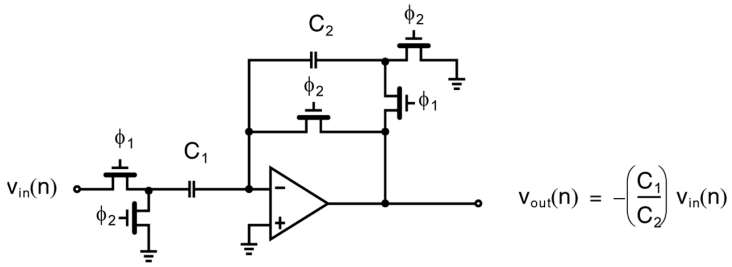
$$H(z) = -\frac{K_3 z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + K_3 - K_2K_5}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)}$$

This transfer function turns out to be better suited for realizing high-Q transfer functions (less spread).

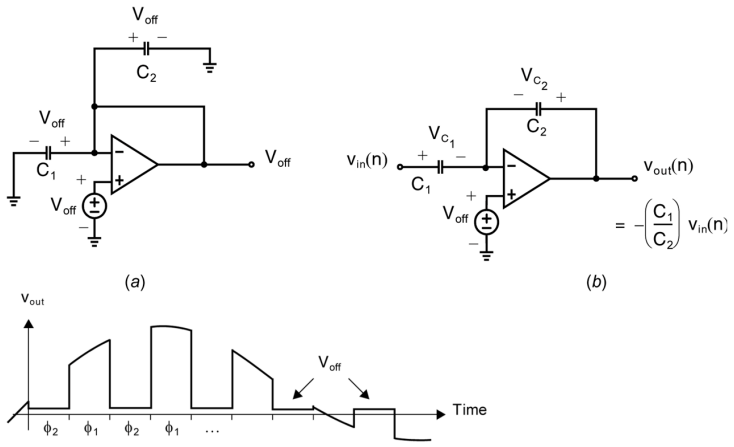


Gain

- Resettable gain circuit
- Samples offset voltage during reset (reduces flicker noise)



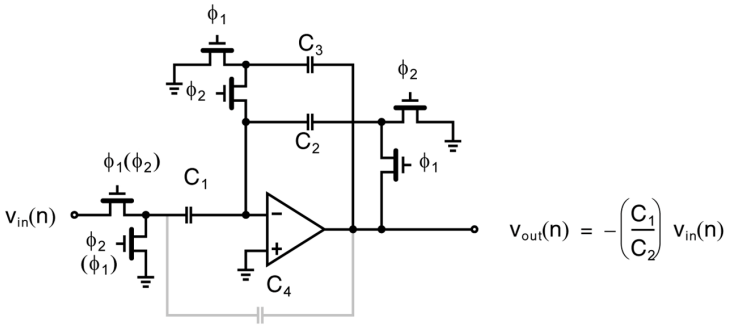
Gain



Amplifier slew-rate requirement is high.

Capacitive-reset gain

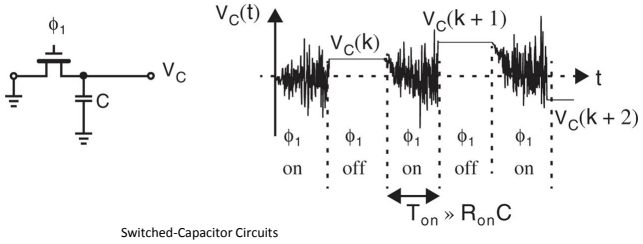
Include a capacitor to hold the output during the reset phase. Avoid excessive slewing. Configurable positive or negative gain.



Noise

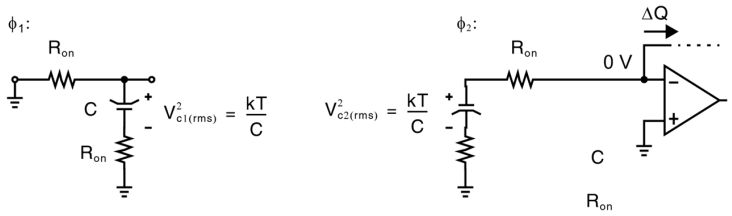
Noise from the switch is sampled on the capacitor with the signal.

Sampling the $\frac{kT}{C}$ noise is like sampling any other signal. The total noise power remains. Broadband noise alias back to the signal band.



Noise

In the delaying parasitic insensitive case, noise is sampled independently in ϕ_1 and ϕ_2, doubling the noise: $\frac{2kT}{C}$

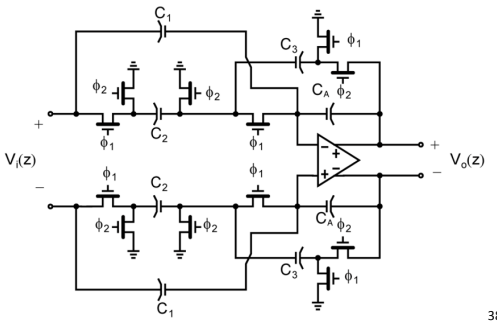


Correlated double sampling (CDS)

- We have already seen how opamp offset voltage can be sampled and canceled.
- Generally, this technique is known as correlated double sampling (CDS)
- Flicker noise is low frequency (assumed to be occurring at lower frequencies than the sampling frequency). Can model it as a randomly varying offset voltage → also canceled
- Can be applied to different sampled systems

Fully differential circuits

Real circuits are almost always fully differential. Coupled noise, power supply noise, substrate noise will mostly affect the common mode, while our signal is in the differential mode. Also, cancels even order harmonics.



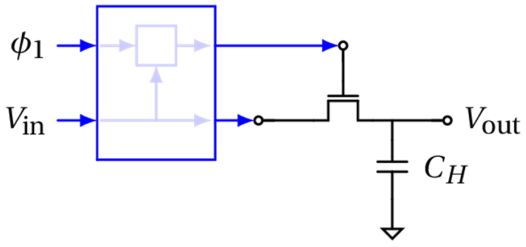
Charge injection

We discussed performance limitation of the switches in the context of sample and hold circuits. The same applies for SC. As we have seen, charge injection limits linearity.

→ arrange the switching and clocking to minimize the signal dependent charge injection.

Bootstrapped switch

Generate a clock voltage such that V_{GS} is constant ($V_{in} + V_{dd}$). Better R_{on} and alleviates charge injection problem. Increased complexity, and reliability can be problematic.



SC amplifier design

Unanswered questions (for now). How do we design amplifiers suitable for SC circuits?

- DC gain (static error)
- GBW (dynamic error)
- PM (stability)
- Slewing requirements
- C_{in} (capacitive divider)
- …

Further reading

Sansen, *Analog Design Essentials,* Springer, 2006, Ch. 17