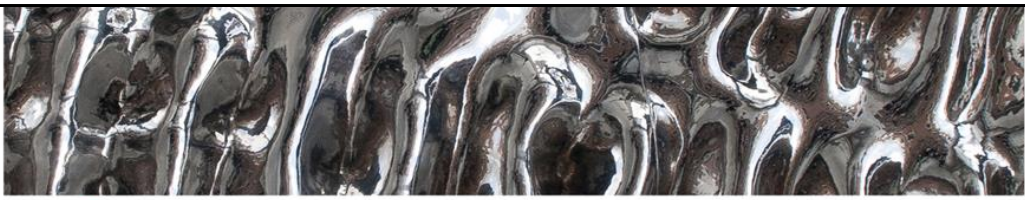

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INF4420

Phase locked loops

Jørgen Andreas Michaelsen
Spring 2013

Outline

- Oscillators
- PLL building blocks
- PLL loop dynamics
- Phase noise

Introduction

Phase locked loops (PLLs) are versatile building blocks used for a range of clocking applications

- Synchronization (deskew)
- Frequency multiplication and synthesis
- Clock and data recovery (serial data)
- Demodulation, etc.

Introduction

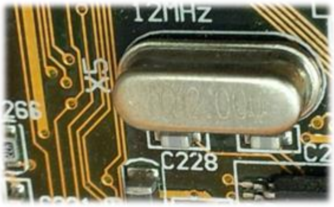
In digital circuits, clocks are used to synchronize computation.

Data converters and discrete time systems use clocks to control the sampling.

Different applications have very different requirements with respect to accuracy and stability (jitter in sample and hold, timing violations, bit error rate (BER), etc.)

Introduction

Most applications use a crystal oscillator. Excellent frequency accuracy and stability (noise and temperature), but "low" frequency only and high cost.

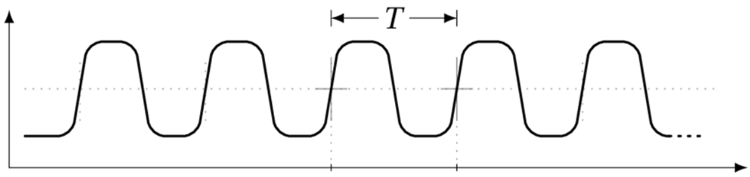


Recently MEMS based oscillators are emerging. Driven by lower cost and smaller size.

Introduction

We begin by discussing voltage controlled oscillators (VCOs).

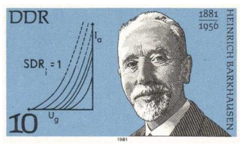
The PLL is a feedback loop that controls the VCO such that its output frequency (or phase) is locked to a reference clock, such as a crystal.



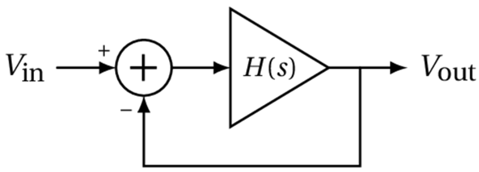
Oscillators

Several possibilities for implementing oscillators in CMOS, such as switched capacitor, relaxation oscillators, LC oscillators, etc.

A popular choice is ring oscillators—*n* delay elements in series with feedback. No stable state. Delay elements may be single ended (such as inverters) or differential (either pseudo or fully differential). High speed, limited by gate delay.



Oscillators



$$\frac{V_{out}}{V_{in}} = \frac{H(s)}{1 + H(s)}$$

Barkhausen stability criterion ⟶

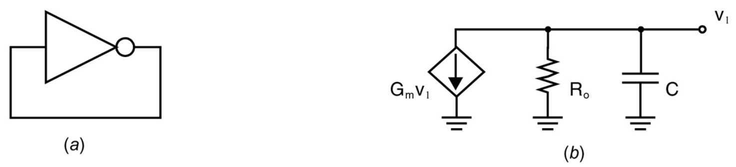
$$|H(j\omega_0)| \geq 1$$

$$\angle H(j\omega_0) = \pi$$

- No known sufficient criteria for oscillation
- Barkhausen stability criterion is necessary but not sufficicent

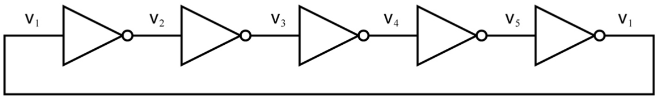
Ring oscillators

A single inverter does not oscillate because its gain is $\ll 1$ when the phase shift is $180°$

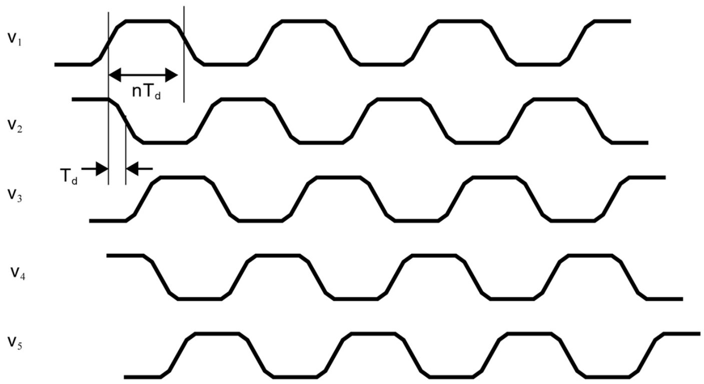


Two inverters have two stable operating points

Ring oscillators



$$f_0 = \frac{1}{2n\tau}$$



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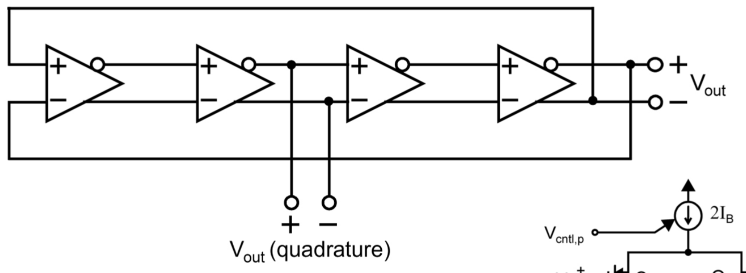
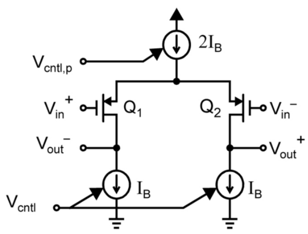
Fully differential ring oscillators





- Reject supply and substrate noise (CMRR and PSRR)
- Even number of stages possible
- No rail to rail swing

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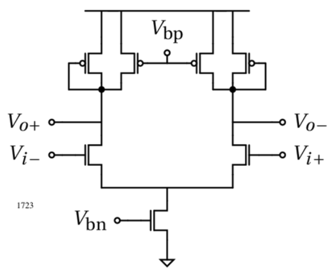
Fully differential ring oscillators

A popular choice for implementing the fully differential delay cell



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 31, NO. 11, NOVEMBER 1996 1723

Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques

John G. Maneatis

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 44, NO. 4, APRIL 2009 1121

Next Generation Intel® Core™ Micro-Architecture (Nehalem) Clocking

Nasser Kurd, *Member, IEEE*, Praveen Mosalikanti, Mark Neidengard, *Member, IEEE*, Jonathan Douglas, and Rajesh Kumar

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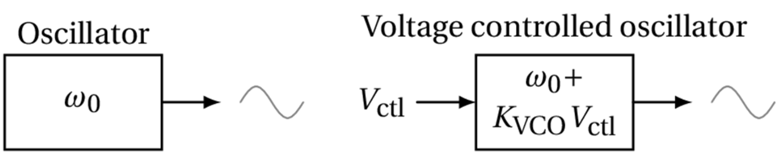
Voltage controlled oscillators (VCOs)

Control voltage, V_{ctl}, is used to generate biasing of the oscillator to modulate the output frequency.

In most practical cases we are using the control voltage to modulate the biasing current (V/I).



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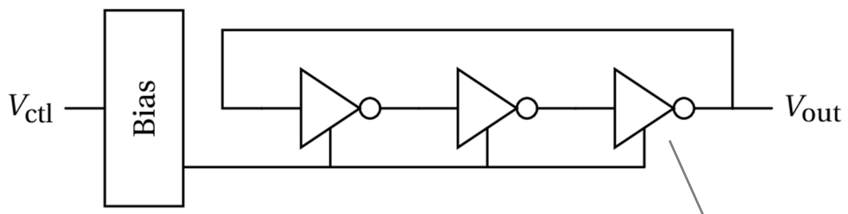
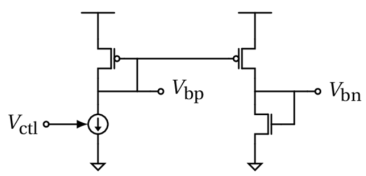
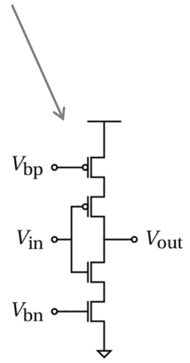
Voltage controlled oscillators (VCOs)



Starved inverter VCO example:





Voltage controlled oscillators (VCOs)

Typical specifications

- Tuning range
- Linearity, ω_{out} vs. V_{ctl}
- Amplitude
- Power consumption
- CMRR and PSRR
- Jitter (phase noise)
- …

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Oscillator model

We model the oscillator in terms of phase, ϕ. Later when we discuss the full PLL we model the phase response of the system.

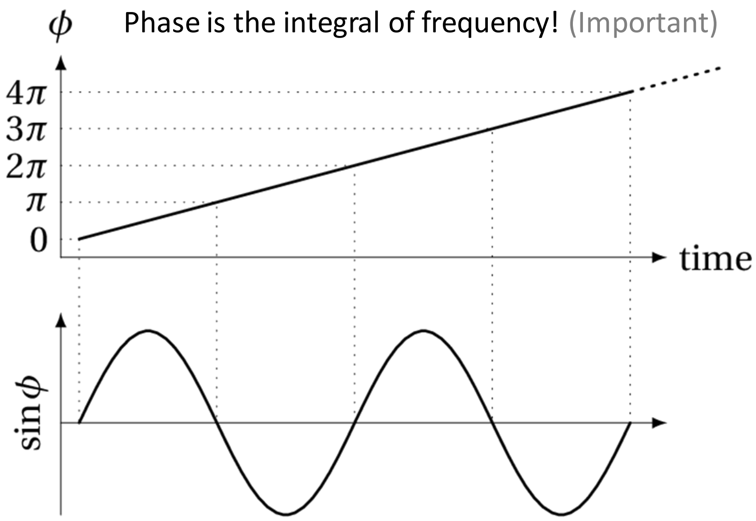
Without loss of generality, we assume a sine wave output of the oscillator (can be any periodic function)

$$V_{osc}(t) = E \sin(\omega_0 t + \phi(t))$$

Free running (fixed) frequency

Instantaneous phase

Oscillator model



Oscillator model

Instantaneous output frequency

$$\omega_{inst}(t) = \frac{d(\omega_0 t + \phi(t))}{dt} = \omega_0 + \frac{d\phi}{dt}$$

Deviation from the free running frequency

$$\omega(t) \equiv \omega_{inst}(t) - \omega_0 = \frac{d\phi}{dt}$$

Oscillator model

$$\phi(t) = \phi(0) + \int_0^t \omega(\tau)\, d\tau$$

Arbitrary initial phase

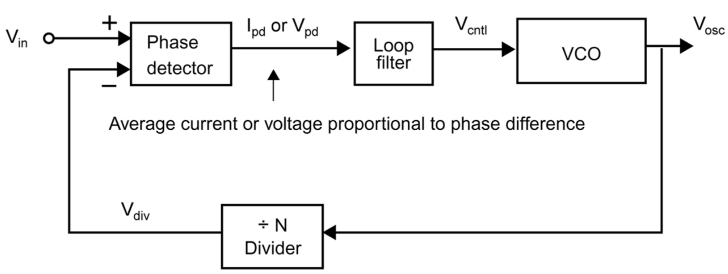
Laplace transform:

$$\phi(s) = \frac{\omega(s)}{s} = \frac{K_{osc} V_{ctl}(s)}{s}$$

K_{osc} is a mapping from the control voltage to the frequency deviation. Assumed to be constant.

Phase locked loop (PLL)

The PLL is a closed loop feedback system that drives the control voltage of the VCO, "locking" its phase to a reference phase, by continuously comparing the phase. V_{in} is a reference clock. The divider is needed if we want the output frequency multiplied.



Phase locked loop (PLL)

- Needed because the output frequency of the VCO is unpredictable—sensitive to the PVT condition. Also, noise causes the phase to drift.
- I.e. we can not simply “program” a control voltage and know what the output frequency is.
- Or needed because we want to synchronize two clocks in some applications (zero crossings occurring at the same time instants)
- Or if we want to demodulate the input signal …

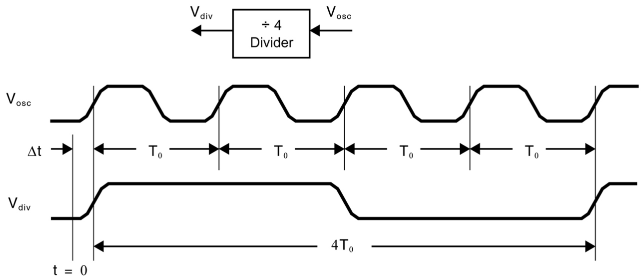
Phase locked loop (PLL)

We will first study how each PLL building block works and how we can model it in terms of phase

- VCO (already covered)
- Divider
- Phase detector
- Loop filter

We then model the PLL as a system

Clock divider (DIV)



Easy to divide by 2^N. Fractions are also possible.

The division is constant, thus:

$$\phi_{div}(s) = \frac{\phi(s)}{N}$$

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Phase detector (PD)

- Generate an output voltage or current where the (average) value is proportional to the phase difference
- Two inputs, the reference clock (REF) and the (divided) VCO clock.

Several possibilities for implementing the PD, but the so called charge pump PD is the most common. Many variations of the charge pump PD.

Linear PD

Multiplying PD,

$V_{pd} = K_M V_{in} V_{div}$

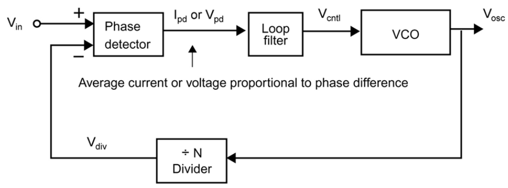
$V_{in} = E_{in} \sin \omega t$

$V_{div} = E_{div} \cos(\omega t - \phi_d)$

$\sin A + \cos B = \frac{1}{2}(\sin(A+B) + \sin(A-B))$

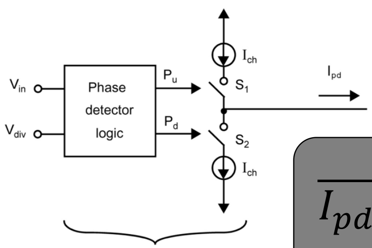
$$\rightarrow V_{pd} = K_M \frac{E_{in}E_{div}}{2}(\sin \phi_d + \sin(2\omega t - \phi_d))$$

$$V_{cntl} = K_{lp}K_M \frac{E_{in}E_{div}}{2} \sin \phi_d \approx \boxed{K_{lp}K_{pd}\phi_d}$$



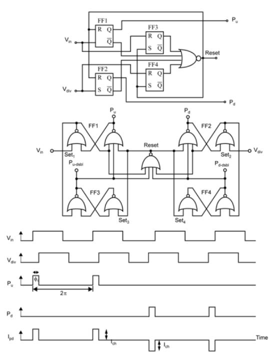
Charge pump PD

Generate a pulsed output who's pulse width is equal to the phase difference (ϕ_d). If REF comes first the VCO must speed up. Otherwise the VCO must slow down.



Charge-pump phase detector

$$\boxed{\overline{I_{pd}} = I_{ch}\frac{\phi_d}{2\pi}}$$

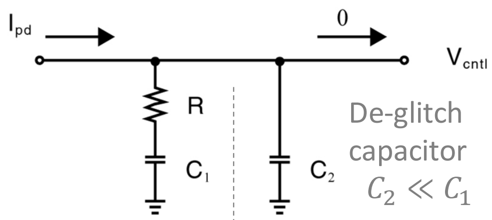


Loop filter (LP)

- Smooth out the pulses from the PD
- Usually, current input (from the PD) and voltage output (VCO control voltage) → F^{-1}
- Important for the overall PLL transfer function
- Again, several possibilities … Active vs. passive, first order vs. second order.

Loop filter (LP)

$$\frac{V_{cntl}(s)}{I_{pd}(s)} = \frac{Z_1(s)Z_2(s)}{Z_1(s)+Z_2(s)} = \frac{1+C_1Rs}{s(C_1+C_2+C_1C_2Rs)}$$



$Z_1 = R + \frac{1}{sC_1}$ $Z_2 = \frac{1}{sC_2}$

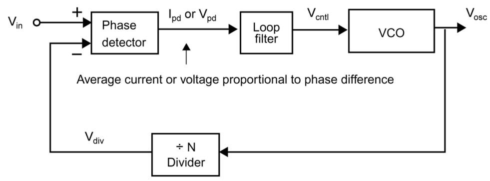
Simplify this as:

$$\frac{V_{cntl}(s)}{I_{pd}(s)} = K_{lp}H_{lp}(s) \approx \frac{1}{C_1}\frac{1+sRC_1}{s}$$

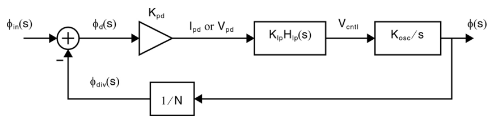
$K_{lp} = C_1^{-1}$
$\omega_z = (RC_1)^{-1}$

Small signal PLL model

We now have small signal models for all components.



We use this to model the full feedback system in terms of a Laplace description of the phase and derive the system transfer function.



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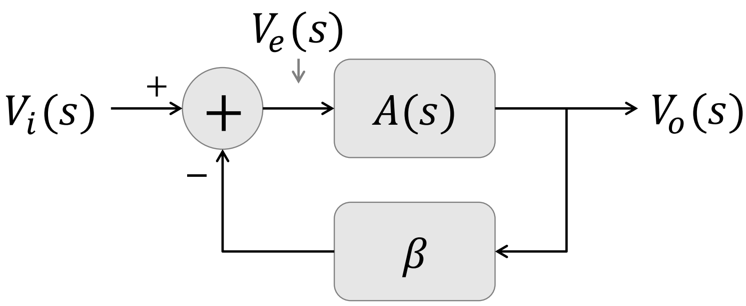
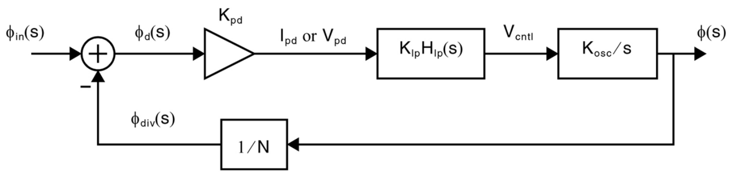
Small signal PLL model



$$H_o(s) = \frac{V_o(s)}{V_i(s)} = \frac{A(s)}{1 + \beta A(s)} \quad H_e(s) = \frac{V_e(s)}{V_i(s)} = \frac{1}{1 + \beta A(s)}$$

Small signal PLL model



$$A(s) = \frac{K_{pd}K_{lp}H_{lp}(s)K_{osc}}{s}, \qquad \beta = \frac{1}{N}$$

Phase difference (error) transfer function

$$\frac{\phi_d(s)}{\phi_{in}(s)} = \frac{1}{1+\beta A(s)} = \frac{Ns}{K_{pd}K_{lp}H_{lp}(s)K_{osc} + Ns}$$

Small signal PLL model

The DC gain of $\frac{\phi_d}{\phi_{in}}$ is zero: The phase difference converges towards zero, which is what we want.

$$\omega_{pll} \equiv \sqrt{\frac{K_{pd}K_{lp}K_{osc}}{N}}, K_{lp}H_{lp}(s) = K_{lp}\left(\frac{1}{s} + \frac{1}{\omega_z}\right)$$

$$\frac{\phi_d(s)}{\phi_{in}(s)} = \frac{1}{\omega_{pll}^2} \cdot \frac{s^2}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{pll}^2}}$$

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Small signal PLL model

Similarly we find the output transfer function

$$H(s) = \frac{\phi(s)}{\phi_{in}(s)} = \frac{A(s)}{1 + \beta A(s)} = \frac{NK_{pd}K_{lp}H_{lp}(s)K_{osc}}{K_{pd}K_{lp}H_{lp}(s)K_{osc} + Ns}$$

$$H(s) = N\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_z} + \frac{s^2}{\omega_{pll}^2}}$$

Second order denominator

$$1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}$$

Resonant frequency

$$\omega_0 = \omega_{pll}$$

$$Q = \frac{\omega_z}{\omega_{pll}}$$

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Small signal PLL model

- $\omega_z > \omega_{pll}$ underdamped, transient oscillations
- $Q = 0.5 \rightarrow H(s) = N\frac{1+\frac{s}{\omega_z}}{\left(1+\frac{s}{\omega_{pll}}\right)^2}$,
  $\omega_z = \frac{\omega_{pll}}{2}, \omega_{3dB} = 2.5\omega_{pll}$
- $Q \ll 0.5$, requires a low frequency ω_z, which implies large passive component values.

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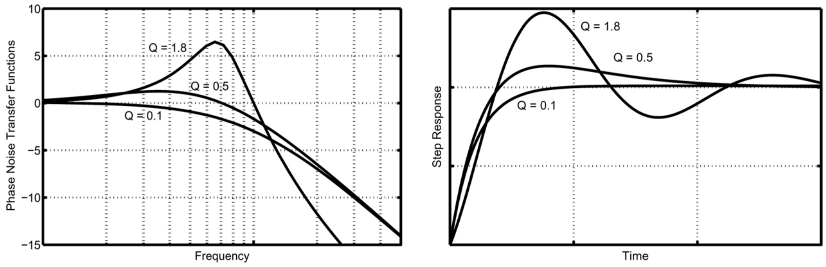
Small signal PLL model



(a) (b)

The book outlines a basic design procedure (19.2.3)

$Q = 0.1$ and $Q = 0.5$ are reasonable choices, depending on the application.

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Small signal PLL model

The small signal model does not capture all aspects of the system. We must be aware of the limitations, including

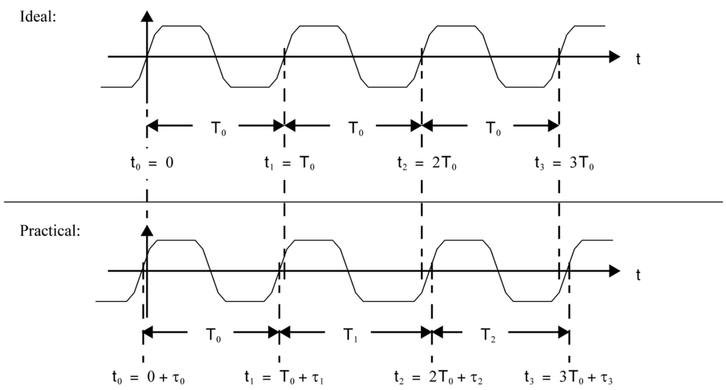
- Large signal lock. What happens before the small signal model is valid? How long does it take to achieve lock? Is the PLL able to achieve lock?
- The PLL is discrete time, but we model it as continuous time (e.g. the phase detector)

Non-ideal circuit properties

- The charge pump phase detector does not track when the phase difference is small because of finite rise and fall times
- Mismatch in the up and down current due to timing or current source impedance
- Power supply coupled noise, random and deterministic jitter
- …

Jitter and phase noise

Ideally, the k-th zero crossing of the clock is at $t_k = kT_o$



Clock *signal* is conveyed by the timing of the *zero crossings* relative to some reference voltage level, or the *phase*.

Jitter and phase noise

However, noise introduces a random deviation from the ideal zero crossing time points

$$t_k = kT_0 + \tau_k$$

τ_k is the absolute jitter. Can also be expressed in radians

$$\phi_k = \tau_k \frac{2\pi}{T_0}$$

Jitter and phase noise

We define phase noise, $S_\phi(f)$, as the power spectral density of the sequence ϕ_k.

$$\sigma_\tau^2 = \left(\frac{T_0}{2\pi}\right)^2 \int_0^{\frac{1}{2T_0}} S_\phi(f)\, df$$

$S_\phi(f)$ is $\frac{\mathrm{rad}^2}{\mathrm{Hz}}$

Period jitter

Rather than looking at the jitter in terms of absolute jitter, the absolute time of the zero crossings, we can look at the length of the clock periods:

$$T_k = t_{k+1} - t_k = T_0 + \tau_{k+1} - \tau_k$$

Period jitter

Deviation of the period from the nominal value, T_0

$$J_k = T_k - T_0 = \tau_{k+1} - \tau_k$$

The period jitter is the differentiation of the absolute jitter, $z - 1$

$$\sigma_J^2 = \left(\frac{T_0}{\pi}\right)^2 \int_0^{\frac{1}{2T_0}} \sin^2(\pi f T_0)\, S_\phi(f)\, df$$

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P-Cycle jitter

Rather than looking at the deviation in one clock period, we now look at the variation in a duration defined by P clock periods—P-cycle jitter

$$J(P)_k = t_{k+P} - t_k - PT_0 = \tau_{k+P} - \tau_k$$

$$\sigma^2_{J(P)} = \left(\frac{T_0}{\pi}\right)^2 \int_0^{\frac{1}{2T_0}} \sin^2(\pi f P T_0)\, S_\phi(f)\, df$$

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Adjacent period jitter

The difference between the length of two adjacent periods

$$J_{k+1} - J_k = (T_{k+1} - T_0) - (T_k - T_0)$$

This implies double differentiation of the absolute jitter, $(z-1)^2$

$$\sigma^2_C = \left(\frac{2T_0}{\pi}\right)^2 \int_0^{\frac{1}{2T_0}} \sin^4(\pi f T_0)\, S_\phi(f)\, df$$

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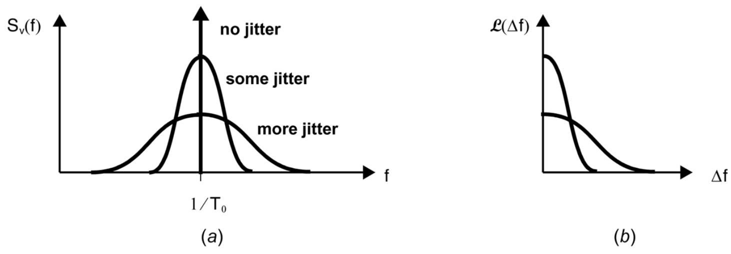
Measuring phase noise

- More practical to measure the (estimated) phase noise rather than the jitter
- Jitter can be calculated from the phase noise
- Phase noise is inferred from the PSD of the clock signal directly, $S_v(f)$
- Baseband noise is mixed up by the carrier
- Spectrum analyzers usually have a phase noise measurement option

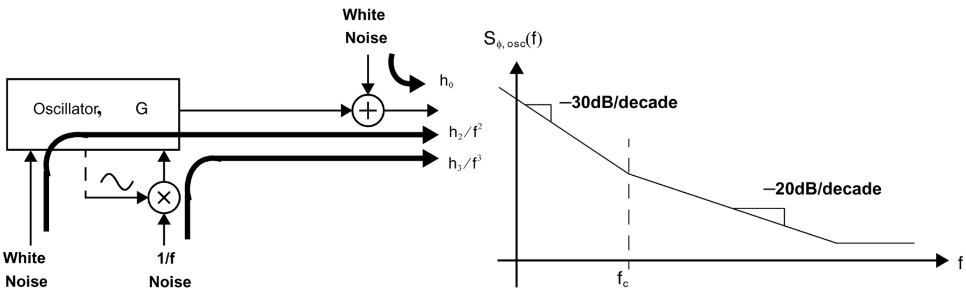
Measuring phase noise



$$\mathcal{L}(\Delta f) = \frac{S_v\left(\frac{1}{T_0} + \Delta f\right)}{\frac{A^2}{2}}, \qquad \mathcal{L}(\Delta f) \equiv \frac{S_\phi(\Delta f)}{2}$$

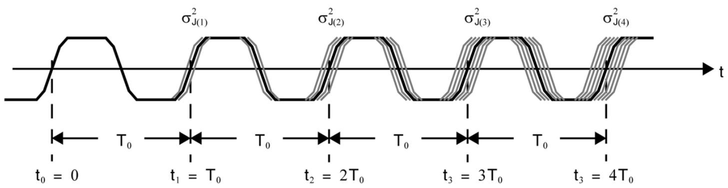
Oscillator phase noise

- The integrating nature of the oscillator accumulates the noise
- Flicker noise is now f^{-3} and white noise is f^{-2}



Oscillator phase noise in the time domain

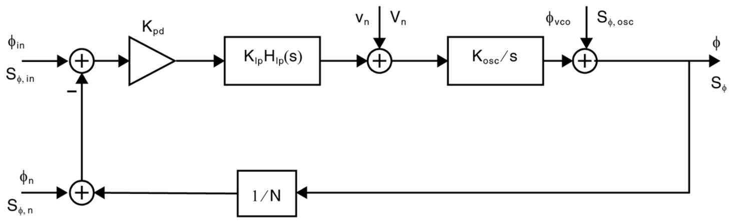
- In the time domain, the jitter accumulates
- A “noise event” remains for all subsequent time. There is no restoring force acting on the oscillator



Jitter and phase noise in PLLs

All PLL components generate noise and influence the overall PLL jitter, including the reference clock.

We use small signal transfer functions to find the noise influence on the PLL output.



Reference and divider phase noise

- We already know the transfer function from the PLL input to the PLL output, $H(s)$
- Divider output and reference are connected to the PLL input
- Lowpass transfer function

PLL VCO phase noise

$$H_{osc}(s) = \frac{\phi(s)}{\phi_{vco}(s)} = \frac{Ns}{K_{pd}K_{lp}H_{lp}(s)K_{osc} + Ns}$$

The VCO noise transfer function is *highpass*, thus the VCO phase noise is suppressed inside the PLL bandwidth. I.e. the feedback loop is tracking and correcting the VCO phase noise.

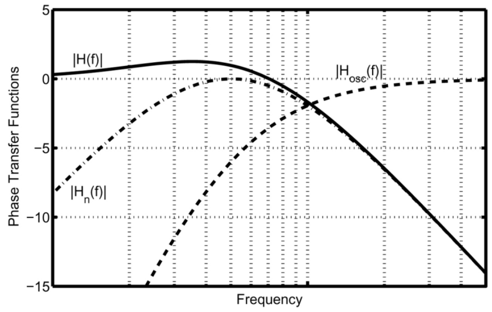
Charge pump and loop filter noise

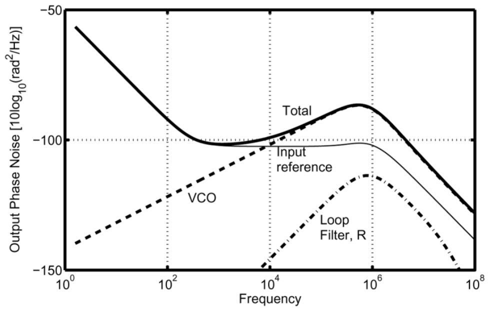
$$H_n(s) = \frac{\phi(s)}{V_n(s)} = \frac{NK_{osc}}{K_{pd}K_{lp}H_{lp}(s)K_{osc} + Ns}$$

Noise injected at the output of the loop filter is *bandpass* filtered on the output of the PLL

Total PLL phase noise

$$S_\phi(f) = S_{\phi,in}(f)|H(f)|^2 + V_n^2(f)|H_n(f)|^2 + S_{\phi,osc}(f)|H_{osc}(f)|^2$$





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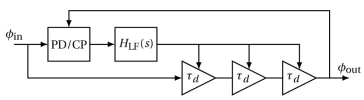
Delay locked loop (DLL)

In certain applications we can use a delay locked loop instead. Using a delay line rather than a VCO.

Phase noise does not accumulate in the delay line, like it does in the VCO. No integration in the delay line, so loop order is one less than the PLL (set by the loop filter). Implications for stability and settling.



Further reading

Gardner, *Phaselock Techniques*, Wiley, 2005

Fischette, *Dennis Fischette's 1-Stop PLL Center*

Kundert, *Predicting the phase noise and jitter of PLL-based frequency synthesizers*, 2012