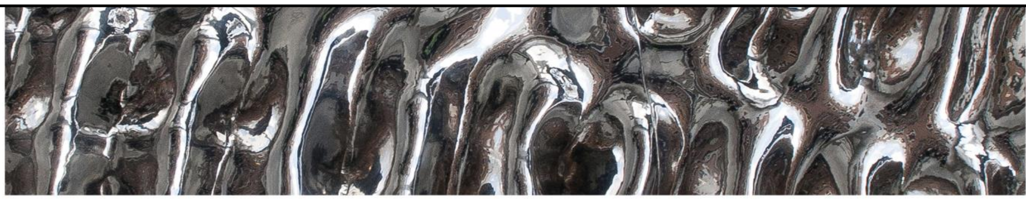

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INF4420

Oversampling Converters

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Outline

- Oversampling and noise shaping
- Single-bit quantization
- Feedback DAC
- Multi-stage noise shaping (MASH)

Introduction

So far we have considered so called Nyquist rate data converters. Operating at sampling rates required to avoid aliasing.

Quantization noise is a fundamental limit.

Improving the resolution of the converter translates to increasing the number of quantization steps (bits): Better component matching, $A_{ol} > \beta^{-1}2^{N+1}$ and $\text{GBW} > F_s \ln 2^{N+1}\pi^{-1}\beta^{-1}$.

Introduction

Instead of relying only on the number of quantization levels, we can use signal processing to improve the resolution. ΔΣ modulator based data converters relies on **oversampling** and **noise shaping** to improve the resolution.

Introduction

Oversampling means that the sampling rate is increased to several times what is required just to avoid aliasing. Shortly, we will see why this helps improving the resolution.

Noise shaping means that the quantization noise is moved away from the signal band that we are interested in. (Oversampling implies that or signal band occupies a fraction of the full spectrum).

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Introduction

We can make high resolution data converters even if the quantizer has few quantization steps (few bits).

However, the data converter must run at higher speed, and requires more complex signal processing. A good fit for CMOS?

Techniques applies to both DACs and ADCs.

Oversampling

Why does oversampling improve resolution?

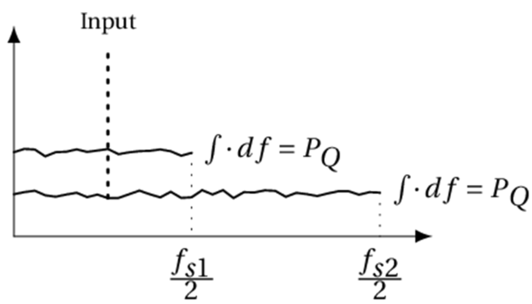
In an ideal data converter, the resolution is limited by the quantization noise, which we (again) assume to be white.

$$P_Q = \frac{\Delta^2}{12}$$

$$\Delta = V_{lsb} = \frac{V_{ref}}{2^N}$$

Oversampling

Important observation: The quantization noise depends on the *quantization step size only*. It does not depend on sampling frequency.



Sampling at a higher frequency reduces the amount of quantization noise inside our signal band.

Oversampling

$$\mathrm{OSR} \equiv \frac{F_s}{2F_b}$$

OSR is the fraction of the full sampled spectrum that our signal band occupies. The quantization noise (that we need to consider) is reduced proportionately. (Assume that we can remove the excess part of the spectrum with a “brick wall” filter).

$$P_Q = \frac{\Delta^2}{12}\frac{1}{\mathrm{OSR}}$$

Oversampling

The signal energy, assuming a full scale sine wave input, is not changed

$$P_S = \frac{\Delta^2 2^{2N}}{8}$$

$$\mathrm{SQNR} = 10\log\frac{P_S}{P_Q} = 6.02N + 1.76 + \underbrace{10\log\mathrm{OSR}}$$

Contribution from oversampling

Oversampling

Doubling the sampling rate improves the resolution by 0.5 bit ($3\ \text{dB} = 10\log_{10} 2$).

Quickly becomes impractical to rely on oversampling only. Sampling rate requirement is too high. We can do better!

Oversampling is almost always used with noise shaping.

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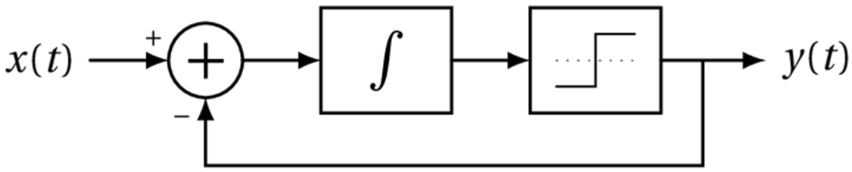
Noise shaping

We can not magically remove noise (fundamental limit). However, we can "move" noise from the signal band to the oversampled part of the spectrum, which we are removing anyway.

The idea is to **highpass filter the noise** (without spectrally shaping the signal). Done correctly, will **suppress noise in the signal band**, at the cost of **amplifying noise in the oversampled** part of the spectrum. (So noise is not moved as such).

Noise shaping

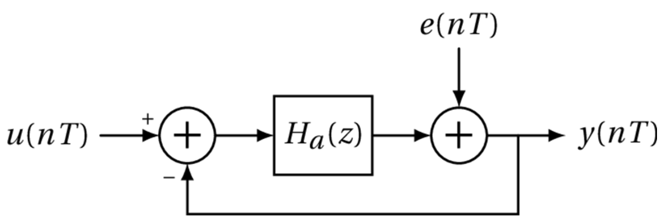
The ΔΣ modulator does noise shaping.



Can be implemented in digital or analog, to implement DACs or ADCs. The analog parts can be continuous or discrete time (switched cap).

Noise shaping

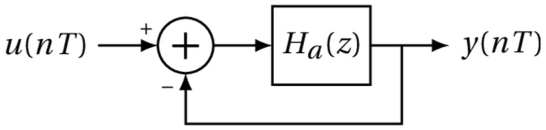
To see how the ΔΣ modulator shapes quantization noise we develop a linearized model.



Two independent inputs: u, the signal, and e, the (white) quantization noise.

Noise shaping

Signal transfer function, STF, $H_s = \frac{Y(z)}{U(z)}$. Analyze by setting the quantization noise input to 0 (superposition).

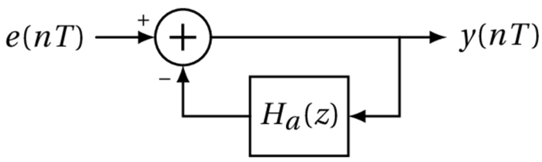


$$Y(z) = H_a(z)[U(z) - Y(z)]$$

$$H_s(z) = \frac{Y(z)}{U(z)} = \frac{H_a(z)}{1 + H_a(z)}$$

Noise shaping

Noise transfer function, NTF, $H_n(z) = \frac{E(z)}{Y(z)}$

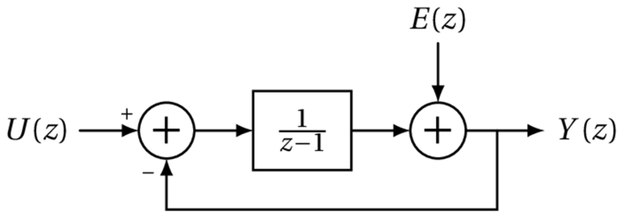


$$Y(z) = E(z) - H_a(z)Y(z)$$

$$H_n(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H_a(z)}$$

Noise shaping

If we choose $H_a(z)$ to be an integrator …

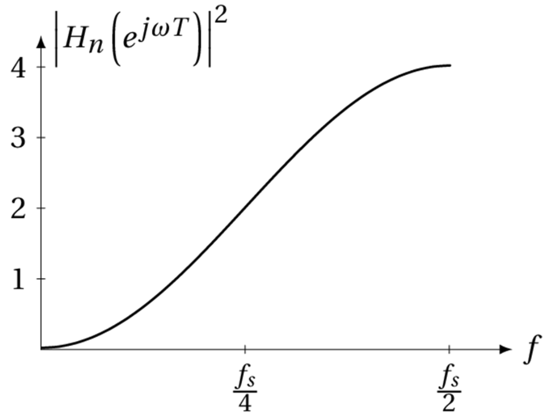


$H_s(z) = z^{-1}$ ← Simple delay (signal)

$H_n(z) = 1 - z^{-1}$ ← Highpass filter (noise)

Noise shaping

NTF frequency response



The NTF shapes the quantization noise.

At low frequencies the quantization noise is suppressed.

$$H_n\left(e^{j\omega T}\right) = 1 - e^{-j\omega T}$$
$$= 2je^{-\frac{j\omega T}{2}} \sin\frac{\omega T}{2}$$

Noise shaping

$$P_Q = \int_0^{f_b} \frac{2f}{f_b}\frac{\Delta^2}{12} \cdot \underbrace{4\sin^2\frac{\pi f}{f_s}}_{\text{NTF}} df$$

$$\approx \left(\frac{2f_b}{f_s}\right)^3 \frac{\pi^2}{3}\frac{\Delta^2}{12}$$

Noise shaping

Assuming a full-scale sine wave input as before

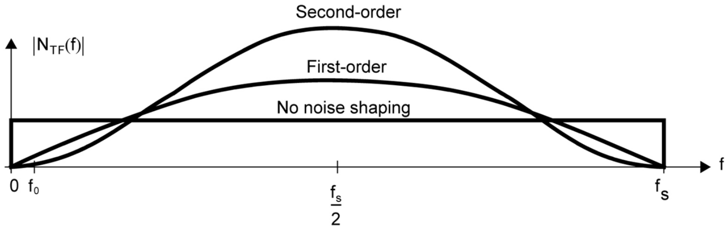
$$\text{SQNR} = 6.02N + 1.76 - 5.17 + 30\log_{10}\text{OSR}$$

Doubling the OSR improves the SQNR by 1.5 bits.
(compared to oversampling only, 0.5 bits).

Second order noise shaping

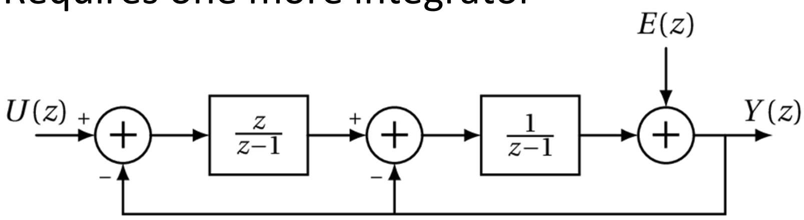
We can design the modulator such that it achieves a second order highpass filter instead.

More suppression in the signal band (assuming sufficient OSR).

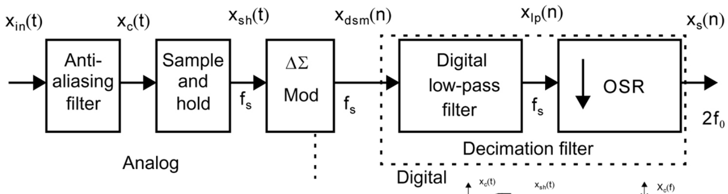


Second order noise shaping

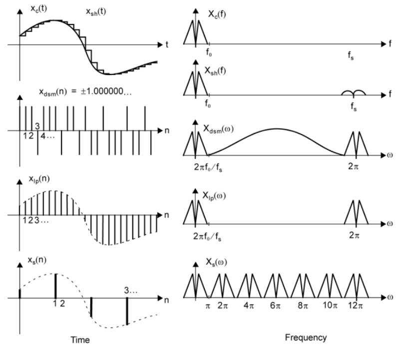
Requires one more integrator



ΔΣ modulator based ADC



Need post processing of the ΔΣ modulator output to reject the oversampled part of the spectrum (decimation)



Decimation

- Usually the decimation is performed in multiple stages
- Filters with low hardware complexity at the highest sampling rates: sinc filters does not need multipliers, just delay and addition.
- More accurate filters at lower frequencies, can compensate for droop introduced by the sinc filters. Specialized FIR filters for decimation. Half band FIR: every other coefficient is zero.

Single bit quantization

Since we can realize high resolution converters with few quantization levels, why not use a single bit quantizer?

→ Ideally perfectly linear

However, …

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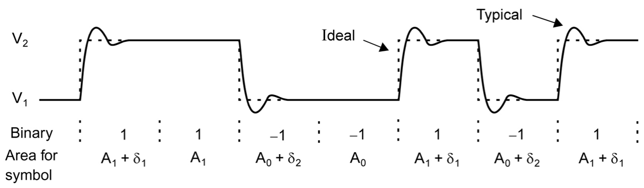
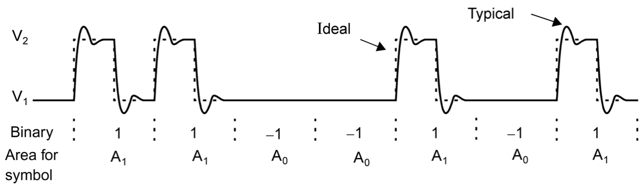
Single bit quantizer linearity

Average value depends on the sequence of bits



Return to zero coding to eliminate memory effect



Still need stable reference levels …

Single bit quantizer linearity

We assumed the quantization noise was white (to model the system)

This assumption is not true. The one bit quantizer is a highly non-linear element.

Implications for stability and output spectrum.

588 IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. 37, NO. 6, JUNE 1989

Spectral Analysis of Quantization Noise in a Single-Loop Sigma-Delta Modulator with dc Input

ROBERT M. GRAY, FELLOW, IEEE

956 IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. 37, NO. 9, SEPTEMBER 1989

Quantization Noise in Single-Loop Sigma-Delta Modulation with Sinusoidal Inputs

ROBERT M. GRAY, FELLOW, IEEE, WU CHOU, STUDENT MEMBER, IEEE, AND PING W. WONG, STUDENT MEMBER, IEEE

Idle tones

Sine or DC input and single bit quantization gives rise to quantization noise that is not white. Some inputs cause the output pattern to repeat after a deterministic number of samples.

Shows up as tones in the output spectrum and may occur inside the signal band.

Intentionally add noise to decorrelate the quantization noise pattern, *dithering.*

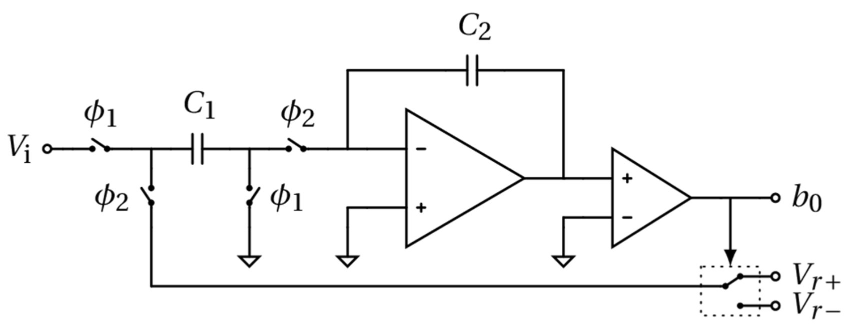
Stability

We modeled the quantizer as a linear addition, but the single bit quantizer is highly non-linear. *Implications for stability*. The quantizer can be overloaded—meaning its input is outside the allowed/expected range, giving quantization errors beyond $\pm\frac{\Delta}{2}$. Stability is not well understood. A practical choice is to ensure

$$\left|H_N\left(e^{j\omega}\right)\right| \leq 1.5$$

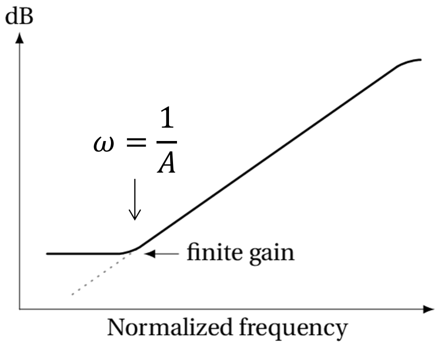
Circuit example

First order ΔΣ modulator discrete time implementation example (single bit quantizer).



Finite amplifier gain

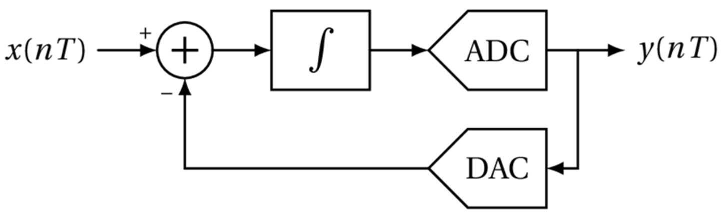
The integrator transfer function is influenced by finite amplifier gain. By implication, *this affects the noise shaping.*



The integrator pole shifts from DC to $z = 1 - 1/A$. Limits noise suppression at low frequencies. In this region, doubling the OSR gives 0.5 bit (no benefit from noise shaping)

Multi-bit quantization

Multi-bit quantization helps stability and idle tones. Less inherent quantization noise. Quantizer non-linearity is shaped by the NTF, but the DAC must be linear to the full resolution of the system.



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Multi-bit quantization

Need techniques to deal with severe DAC linearity requirements

- Dynamic element matching (DEM)
- Calibrating current sources
- Digital calibration
- Combining single and multi-bit feedback

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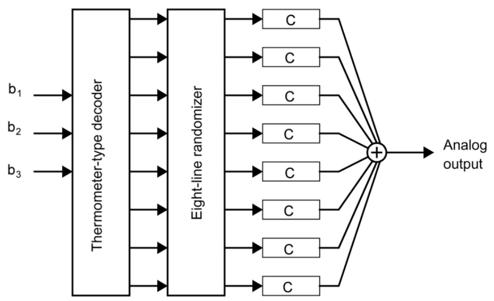
Dynamic element matching

Randomize DAC component selection (current sources, capacitors, ...). Ideally, turns the non-linearity into white noise.

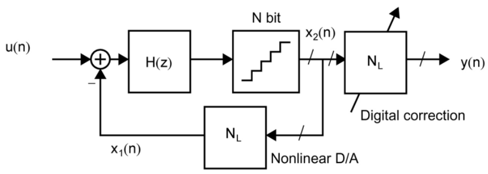


Current source calibration

Current source (CS) DACs are a common choice for the feedback DAC. We can make the current sources programmable to compensate for the non-linearity.

Digital calibration

Include some digital function that maps the output of the converter. Can compensate by generating the inverse of the ADC non-linearity. Reconfigure the converter temporarily to a single bit system to generate the reference levels. Several digital calibration schemes are possible.



Higher order noise shaping

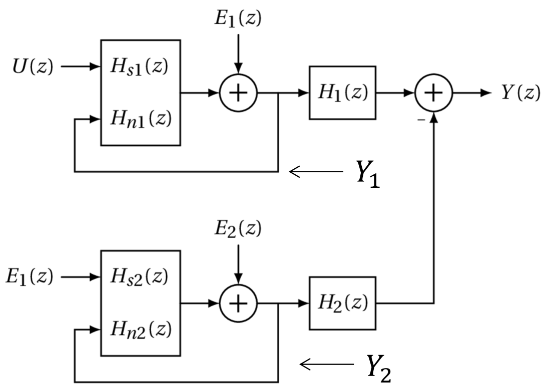
Increasing the order of the noise shaping further attenuates the noise in the signal band

Doubling the OSR improves the resolution by $L + 0.5$ bit, where L is the order of the modulator.

Stability is a concern for higher order modulators. (Unlike increasing the number of quantization levels, which helps stability).

Multi-stage noise shaping (MASH)

A cascade structure where a higher order modulator is realized by two lower order modulators.



Input to the second modulator is the quantization noise from the first modulator.

Multi-stage noise shaping (MASH)

We want to cancel the quantization noise from the first modulator.

$$Y_1(z) = H_{s1}(z)U(z) + H_{n1}(z)E_1(z)$$
$$Y_2(z) = H_{s2}(z)E_1(z) + H_{n2}(z)E_2(z)$$
$$Y(z) = H_1(z)Y_1(z) - H_2(z)Y_2(z)$$

Choose $H_1(z)$ and $H_2(z)$ such that $E_1(z)$ cancels.

$$H_1(z)H_{n1}(z) - H_2(z)H_{s2}(z) = 0$$

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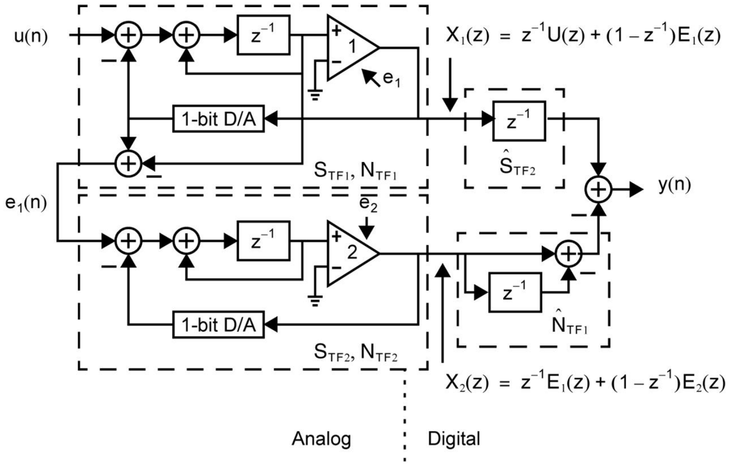
Multi-stage noise shaping (MASH)

This requirement is satisfied if we choose

$$H_1(z) = H_{S2}(z) \text{ and } H_2(z) = H_{N1}(z)$$

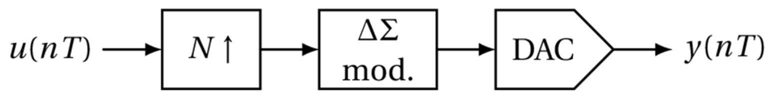
Easy enough, but we must take into account that $H_1(z)$ and $H_2(z)$ are in digital and we must match them to $H_{S2}(z)$ and $H_{N1}(z)$ which are analog functions. Imperfections in the analog circuitry (offset, gain, etc.) will deteriorate the noise suppression.

Multi-stage noise shaping (MASH)



ΔΣ modulator based DACs

Most of the discussion has (implicitly) been about ADCs. The same techniques can be used for DACs.



Interpolation to increase the sampling rate in digital, and the integrator in the ΔΣ modulator is digital rather than analog.

Continuous time ΔΣ

We have assumed sampled data analog processing (switched capacitor).

ΔΣ can also be implemented using continuous time integrators. Can achieve higher speed. (Not part of the curriculum).

Resources

Schreier and Temes, *Understanding Delta-Sigma Data Converters*, IEEE Wiley, 2005